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14. ABSTRACT

In our effort to develop and demonstrate the design, fabrication, and experimental characterization of self-collimation photonic crystal devices (SCPhCs) in both 2D and 3D structures, we identified various tasks and goals towards achieving the proposed applications. Two-dimensional self collimation photonic crystal structures will be used for in-plane optical signal distribution and routing while three-dimensional structures will be used for out-plane signal distribution, to provide high-density optically interconnected optoelectronic PhC circuits to distribute the optical signal between various circuits and in different angles. As previously proposed we intend to fabricate 2D structures using III-V materials and 3D structures using Silicon, and later use flip-chip bonding to construct our optoelectronic circuit. Hence, In this phase we develop and refine III-V lithography and etching processes, including ebeam and UV interferometric lithography, ICP etching, and Oxidation followed by HF undercut. We will also develop suitable growth techniques to obtain GaAs/AlGaAs layered structures for suspended PhC Devices.

15. SUBJECT TERMS
Self collimation, photonic crystals, photonic integrated circuit, chip scale optical interconnect

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Principal Investigator: Dr Dennis Prather

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2 Objectives

2.1 Demonstrate functionality of 2D and 3D self-collimation PhC chip-scale interconnects and characterize their performance

3 Status of Report

The overall objective of this effort is to demonstrate the design, fabrication, and experimental characterization of self-collimation photonics crystal devices for application of high performance electronic warfare systems. This was accomplished by investigating devices that serve the needs of current and future Air Force research programs. To achieve these goals we took a three tiered approach: (1) establish close working relationships with *two* AFRL research teams (one located at Hanscom, AFB, POC Dr. Richard Soref and the other at Wright- Patterson, AFB, POCs Drs. Anthony Crespo and Thomas Nelson); (2) identify and demonstrate the feasibility of suitable nano-photonic devices for rapid commercialization; and (3) explore technologically reaching and novel devices and fabrication processes for next generation photonic band gap technologies. Within the context of our effort we have succeeded in each of these areas and, as a result, are very anxious to continue our strong collaboration with the ARL researchers and the commercialization of nano-photonic devices. Details of each aspect of our approach are presented in the remainder of this report.

4 Accomplishments

A significant early accomplishment in our effort was the establishment of strong collaborative relationships with *two* Air Force research teams, which were centered on applications in Photonic Band Gap devices and systems. A recent meeting was held at the University of Delaware; in attendance were Dr. Antonio Crespo, AFRL/SNDI, and Dr. Dennis Prather, University of Delaware. During the course of the meeting, Dr. Prather gave a presentation on his ongoing research programs at the University of Delaware and highlighted new facilities and equipment added to the current lab infrastructure. The University of Delaware purchased a new MBE system which will facilitate the growth of various materials. Such a system will be highly beneficial to the current effort.

4.1 On-chip Optical Interconnect Concept in Self-Collimating Photonic Crystals

Optical interconnects are considered an attractive approach for global interconnects due to the potential advantages in reduced power consumption and usage of short optical pulses to trigger CMOS circuitry with very precise clocks. The simplest scenario for such a demonstration is to use an off chip optical source, e.g. a VCSEL, and light distribution through waveguides, mirrors and splitters, and conversion through receiver circuitry. This conversion to local electrical clock distribution requires that a minimum power be delivered to a photodetector, which places constraints on the power that can be lost by light distribution from the input optical source to each detector. To date, we recorded the lowest propagation loss in the literature of 1.1 dB/mm using dispersion engineering of slab photonic crystals. Buried coupling, along with three-dimensional dispersion engineering of photonic crystals, would further reduce the propagation loss. Realization of of 2D and 3D

chip-level optical interconnects topologies that are similar materials that achieve better scale of integration and alignment tolerance would be extremely beneficial. Therefore in this effort we propose the development of two such technologies. The first is concerned with creating a single layer of opto-electronic interconnects using planar self-collimation photonic crystal and the second is concerned with developing a full three-dimensional interconnect using buried silicon micromachining techniques. Hence during the project time of this program we will design, fabricate and demonstrate both planar photonic crystal circuits realized in GaAs slab and a buried 3D photonic crystal in silicon. In the case of the slab it will be flip-ship bonded onto an underlying CMOS substrate that contains the appropriate driver and receiver that serve to input and output optical signals to the slab. The slab will also contain optical sources and receivers that serve to generate and detect light. Within the slab we will also include a self-collimation photonic crystal that serves as the interconnect medium between the source and the detector. A representative illustration of this device is shown in Fig. 1(a). In the case of the buried silicon optical interconnect technology, we refer to as the sub-surface silicon optical bus (S3B), we will achieve direct integration into the CMOS process.

Our proposed approach towards such a demonstration is by engineering the dispersion properties of buried silicon three-dimensional photonic crystals to create sub-micron routing channels and control light, as shown in Figure 1. The conceptual rendering in Figure 1depicts a buried photonic-crystal lattice used to route optical signals beneath surface-patterned CMOS electronics. We seek a buried silicon lattice because of the desire to have a PhC fabricated in the handle part of an SOI wafer, enabling the realization of sub-surface silicon optical buses. In this way, CMOS circuits could be fabricated on the topside, sources and emitters can be flip-chip bonded directly on top to emit down through the oxide layer, and optical signals would be subsequently confined in the buried PhC lattice. This would enable the realization of a complete monolithic optical interconnect medium and would only require the flip-chip integration of the active devices, shown (not to scale) atop the structures in Figure 1.

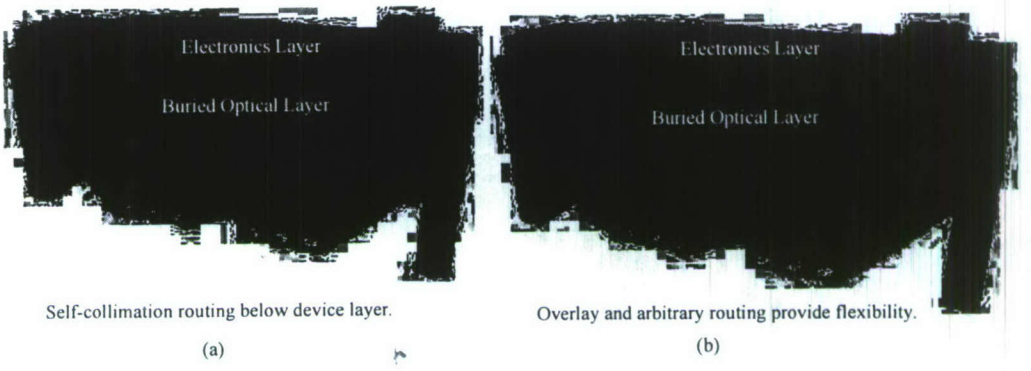


Figure 1: Conceptual rendering of a monolithic integrated optoelectronic device containing a PhC-based sub-surface silicon bus (S3B) for optical routing. The optical bus is comprised of a buried three-dimensional photonic crystal, embedded beneath the electronic device layer. (a) and (b) show different optical paths followed by beams launched into different layers of the S3B, by a source with multiple emitters. The beams are coupled into the bus by angled mirror facets, and the lower beam in (b) is redirected by vertical 45-degree mirrors. The bus and coupling/routing structures will by fabricated by etching from the back side.

Additionally, with a buried lattice, higher interconnect densities and 3D interconnect architectures are possible due to the ability to stack several optically isolated confining levels within the same chip area, and even to route signal beams between levels.

4.1.1 Self collimation in 3D Photonic crystal structures

In the previous report we presented detailed analysis and various applications of self collimation in 2D planar photonic crystal structures. In this report we will expand such analysis to 3D PhC structures. The simplest generalization of dispersion engineering using a square lattice into three dimensions suggests a 3D simple cubic lattice. As it turns out, a simple-cubic Si/air lattice has a small omni-directional photonic band gap as shown in Figure 2; however of greater interest in this context is the fact that it has very profound self-collimation properties.

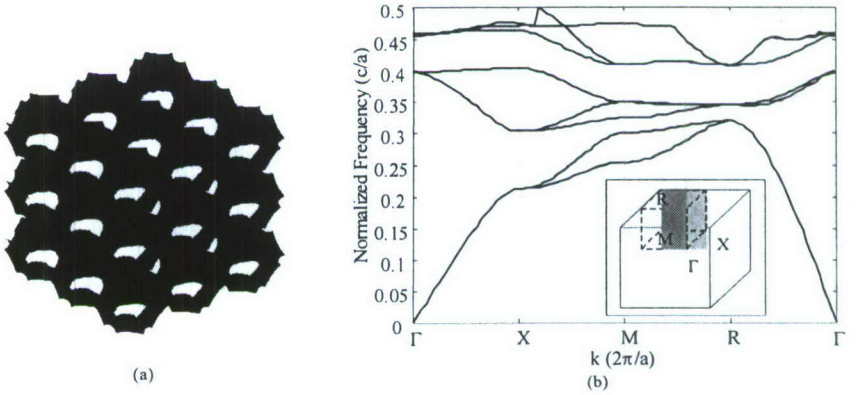


Figure 2: (a) Simple cubic silicon photonic crystals with overlapping spheres; (b) Band diagram along the edge of Brillouin zone. The insets show the schematic view of the high-symmetry points in the first irreducible Brillouin zone.

To understand this, consider a silicon simple cubic PhC (refractive index, $n = 3.5$) as shown in Fig. 2 (a). The sphere radius is r = 0.55 a, in which a is the lattice constant. Since the radius is bigger than 0.5a, the air spheres are actually overlapping with each other. Unlike the planar PhCs in which case the electromagnetic field configurations are bound to the slab by total internal reflection in the vertical direction, in this full 3D PhC case, an electromagnetic wave propagating within the periodic structure obeys the same guiding mechanism in both vertical and lateral directions. The interaction between the electromagnetic wave and the periodic structure is most appropriately interpreted through a dispersion diagram that characterizes the relationship between the frequenciesω, of the wave and its associated wave vector, k.

We calculate the full band diagram for all k-points, instead of only along the perimeter of the irreducible first Brillouin zone. The eigen-frequencies of the discretized bands are functions of wavevector k_x, k_y and k_z. As a result, this allows us to obtain the equal-frequency surface (EFS) of the dispersion diagram for given constant frequency. Figure 3(a) shows the EFS at frequency f = 0.34 c/a; the light- color surface corresponds to the third band and the dark color surface corresponds to the fourth band. Taking cross-section of the EFS at $k_z = 0$, we obtain the equi- frequency contours (EFC) illustrated in Figure 3(b). The solid contour is the third band and the dashed contour is the fourth band. It is clearly shown that the EFC of the third band at frequency f = 0.34 c/a has a flat dispersion surface within a solid angle along the ΓX directions,

which can be used to guide light, while the fourth band does not have such a capability. Since both third and fourth bands are degenerate for the given frequency, when an arbitrary light source is fed into this structure, self-collimation phenomena may not be observed in general. Fortunately, since the eigenmodes for both third and fourth bands are orthogonal, they may be isolated by launching a proper light source, which can be seen from the numerical results presented in Figure 4.

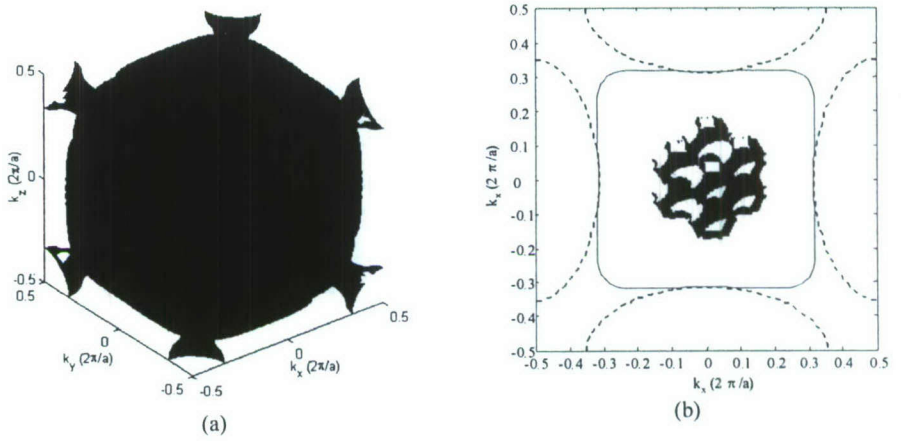


Figure 3: Dispersion relations for the band 3 and band 4 at frequency $f = 0.34\ c/a$. (a) Equal-frequency surface of simple cubic structure, the light color band stands for the third band; the dark color band stands for the fourth band. (b) Equal-frequency contour at $k_z = 0$ plane. The third band has a square-shape EFC, which is suitable for spatial beam routing applications.

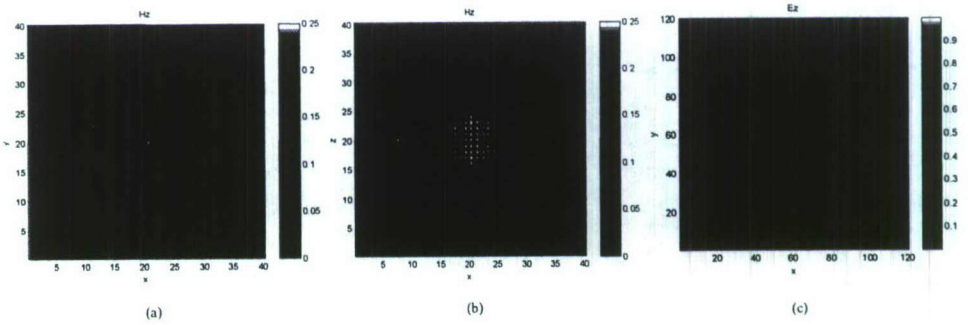


Figure 4: The field distributions of H_z component in the (a) XOY plane and (b) XOZ plane, respectively. (c) Field distribution of E field in XOY plane while an electric dipole source is launched in the center of the simple cubic structure.

To illustrate the self-collimation behavior, we simulated a magnetic dipole source located in the center of a simple cubic structure in silicon, with r/a = 0.55. The Finite-Difference Time-Domain (FDTD) method was applied to analyze this device. The structure was bound by Perfectly Matched Layers (PML) to truncate the computational region and minimize the reflections from the outer boundary. To deal with such a huge computational problem, a PC cluster with 30 nodes, each with 3GHz CPU and 1.5GB memory, was employed.

If we consider the radiation of this dipole in an isotropic medium, an omni- directional radiation pattern will be generated in the XOY plane and an eight-shape pattern in any plane passing through the z-axis . However, in simple cubic photonic crystal at frequency f = 0.34 c/a, the electromagnetic field propagation is restricted to be only along the x, y and z directions due

to the cube shape EFS, when a magnetic dipole source is placed in the center of the cubic PhC structure.

Figures 4 (a) and (b) shows the H_z field component in the XOY and XOZ planes, respectively. The wave is clearly confined within a few lattices, particularly in XOY plane, which is very similar to 2D self-collimation case. The implication of this is that one can experience complete 3D confinement and guiding without the need for a defect within the PhC lattice!

However, if instead of a magnetic dipole source, we introduce an electric dipole source in the simple cubic PhC structure, the wave propagates divergently and no self-collimation phenomenon can be observed, as depicted in Figure 4 (c). This observation is likely related to the orthogonal degenerate modes.

In addition to waveguide-less guiding in these dispersion-engineered 3D PhC simple-cubic lattices, arbitrary routing can be achieved as in their two-dimensional counterparts by etching a rectangular air region in the lattice as shown in Figure 5. Figure 5 depicts a conceptual rendering of air spheres in silicon and routing, similar to Manhattan fabric in electronic circuits, achieved by means of a 45° dielectric mirror. Figure 5 (c) also shows a snapshot of an FDTD electromagnetic simulation demonstrating orthogonal routing.

Applications of fabrication of a device using the 3D PhC dispersion properties are far-reaching in that they hold the potential for dense photonic interconnects with the ability to propagate and route optical beams in an arbitrary fashion with low loss. Having previously demonstrated low-loss propagation in two-dimensional dispersion engineered PhC devices, we are hoping that self-collimation based on three-dimensional PhCs will likewise exhibit low loss. However as of now, it is just a speculation that 3D self-collimation will be low loss. In the following section, we explore the possibility of realizing 3D structures directly in silicon by the use of a planar-mask micromachining process, combined with the prospects of leveraging dispersion guiding via the self-collimation effect.

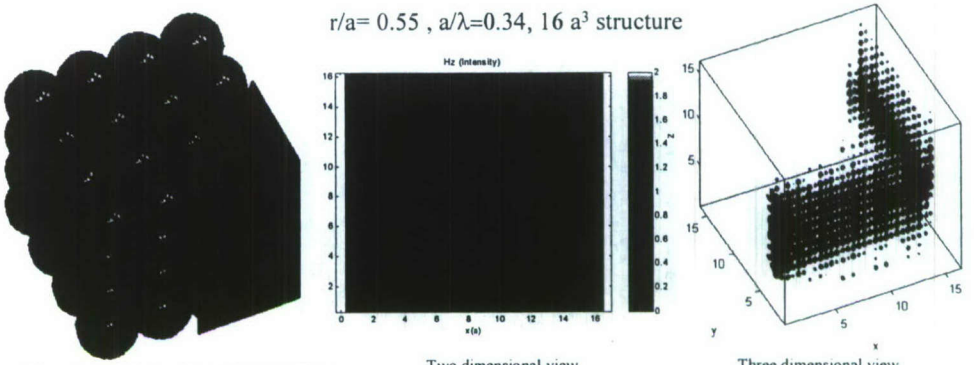


Figure 5: (a) Conceptual rendering of air spheres in silicon, bend is achieved via the 45o air mirror, (b) and (c) Two-dimensional and three-dimensional snapshots respectively of electromagnetic simulations (FDTD) depicting orthogonal routing of light beams.

4.1.2 Fabrication of Three-Dimensional PhCs Using Silicon Micromachining Processes

While 3D photonic crystals have been fabricated using diverse techniques at various length scales, the challenges of disorder, size-dispersion effects, high complexity of multi-step processes, tight alignment tolerances, long turnaround times, and incompatibility with an integrated photonics platform amenable to mass fabrication, leave the scope for new ideas for their fabrication open. TM-DRIE process has been widely used in the fabrication of devices ranging from nanophotonic devices to MEMS to through-wafer optical fiber couplers. In addition, this process indicated the mass fabrication capability over 3" wafers. The next step is to see whether we can leverage the robustness of the TM-DRIE process to sculpt silicon in three-dimensions at the nanoscale.

Hence, in this phase of the proposed effort, we demonstrate a novel fabrication methodology to create 3D simple cubic photonic crystal structures. The proposed approach utilizes conventional silicon micromachining to fabricate three-dimensional photonic crystals. It leverages some of the benefits of layer-by-layer fabrication, such as high index contrast ($n_{Si} \sim 3.5$ vs. $n_{air} \sim 1$), utilization of well established conventional CMOS mass microfabrication technologies, reproducibility, high yield, and compatibility with an optoelectronics platform. However, in contrast to existing layer-by-layer approaches, it is simple, without the complexity, manual-labor intensiveness and long turnaround times of multi-step processes. This process also matches some of the advantages of self-assembly and holographic approaches, namely parallelism, and promises scalability over a wide range of electromagnetic spectrum, from UV to far IR, and further does not require any additional processing, such as backfilling.

Previously, the fabrication of high-fill-factor slab photonic-crystal devices using a time-multiplexed DRIE process by alternating sidewall polymer passivation and silicon etching. The cyclic nature of the process results in rippled sidewalls. By tuning the process parameters, one can control the extremity of the etch. Specifically, one can minimize the size of the ripples and thus attain a smooth, anisotropic profile, as is desired in case of slab photonic crystals; or, one can exacerbate this effect to the point where the ripples become spheres. This effect was first observed during the optimization of the TM-DRIE etch process for high-bandwidth finite-height PhC slab structures, which often requires high fill-factor lattices ($r/a > 0.4$, where r is the hole radius and a the lattice constant). In near-IR slab PhCs in SOI, the lattice constant is around 450 nm. During our investigations, several high-fill-factor slab PhCs were fabricated, and one can notice from Figure 6 that when the diameter of the holes in the mask is nearly equal to the lattice constant, the scallops from the custom etch process started to overlap leading to perforated sidewalls. These ripples can be controlled by adjusting the cycle time and extremity of etching during that cycle of the process. However, by looking at these ripples it seems that it might be possible to exacerbate this effect to the point where they become overlapping spheres. If so, it

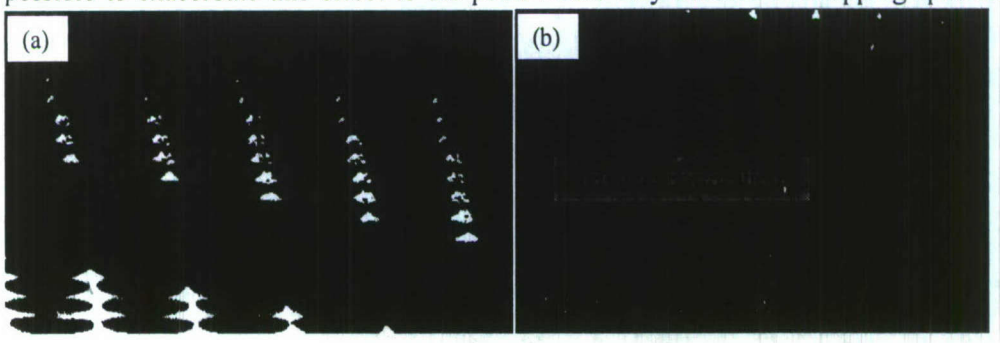


Figure 6: (a) SEM image of an oblique view of an etched high fill-factor slab PhC lattice. Overlapping etch ripples lead to perforated sidewalls. (b) Oblique view of an etched layer of overlapping sphere-shaped voids demonstrating the feasibility of using many such layers to fabricate 3D PhCs.

would be possible to actually realize a buried PhC lattice within a silicon substrate using only a planar etch mask! Assuming that the mask is patterned with a square lattice of holes, this would give rise to a three-dimensional simple-cubic lattice.

In this case, the resulting structure resembles a 3D PhC that would be obtained by infiltrating a matrix of spheres, and the phenomenon is the basis of our proposed process to realize a PhC lattice buried within a silicon substrate. The unique advantage of this process is that it requires only a single surface lithography step followed by an etch sequence. That is, a single etch mask patterned on a substrate suffices for the creation of a complete three-dimensional lattice of a photonic crystal. The etch mask can be patterned by any of the standard lithographic methods, such as deep UV and e-beam lithography. In addition, interference lithography can be used to pattern large areas with near-perfect periodicity and can be applied to the proposed process as a quick and inexpensive alternative to e-beam lithography for the patterning of etch masks as shown in Figure 7.

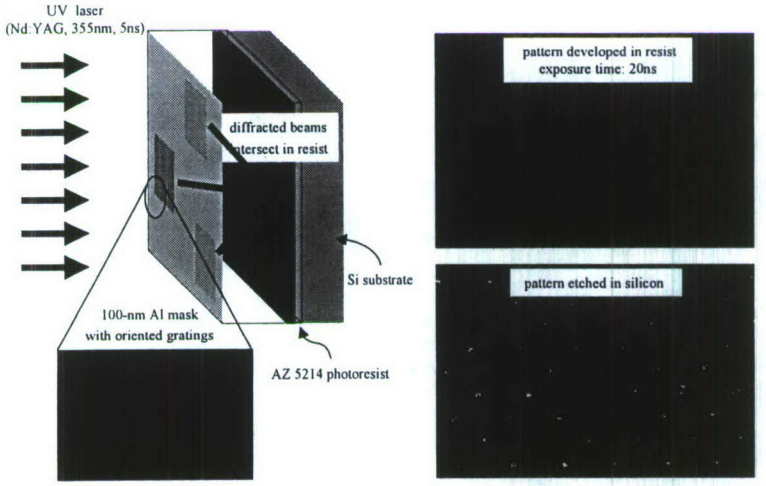


Figure 7: Schematic illustration of interference lithography process developed to fabricate near-IR PhCs in SOI substrates and SEM images of fabricated PhC lattices after lithography and TM-DRIE etch process.

The process follows a similar sequence to DRIE, as shown in Figure 8(a), however, in our case, a considerably longer isotropic etch step is allowed. Thereby spherical voids are opened, which are large enough to overlap, thus perforating side membranes that would otherwise separate them, as shown in Figure 8(a), steps 3 & 6. Following the isotropic etch is the passivation of the spherical surface by depositing a polymer precursor, in this case C_4F_8, which prevents further etching of previously etched features, as in Figure 8(a), steps 4 & 7. The passivation layer is removed locally from the bottom of the spheres by an anisotropic "smash" etch, shown in Figure 8(a), step 5. The etch cycle is then repeated to produce many layers of overlapping spherical voids. If the pattern on the mask is a square lattice of circular openings, the etch sequence yields a 3D structure with simple cubic symmetry, depicted in Figure 8(b).

Further, it is possible to extend the method to enable the fabrication of other crystal structures. For example, using an etch mask with a triangular lattice of holes will yield a simple hexagonal 3D lattice; clearly other similar variations can also be realized. Other structures, such as face-centered and body-centered cubic, can be fabricated using a multilevel etch mask containing interlaced 2D lattices to vertically offset some of the voids. Alternately, vertical offset between sets of voids may be obtained by tilting the sample while etching.

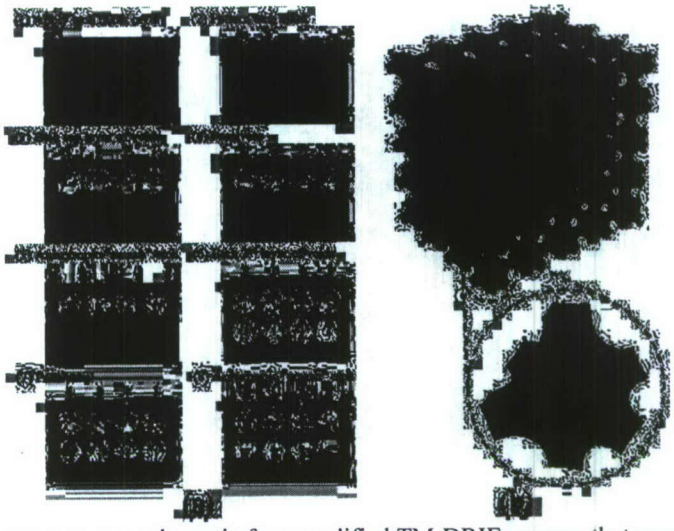


Figure 8: (a) Process sequence schematic for a modified TM-DRIE process that would yield 3D simple cubic PhCs. (b) Rendering of the ideal structure that would result from the etch process depicted in (a). Inset shows the contents of a single unit cell.

Varying the parameters of the isotropic etch step can produce voids which are not spherical, but rather prolate or oblate spheroids. Such symmetry breaking has been shown to lift degeneracies and produce wider band gaps in certain lattices. Conversely, it is also possible to break the symmetry in such a way as to allow independent control of the dispersion in the vertical and horizontal directions, to the point where the complete band gap closes.

The principle advantage and novelty of this technique arises from the use of a planar (2D) etch mask and single cyclic etching process to achieve 3D structures. The proposed process offers the ability to realize high-quality photonic-crystal structures directly in high-index material in a short period of time (seconds to minutes per etch cycle using inductively coupled plasma (ICP) etching system), using a single machine with no interlayer alignment required, while leveraging the mature 2D/planar lithographic methods for the fabrication of the etch mask. In this case, the plasma equipment essentially determines the turnaround time. Since ICP etchers provide a high concentration of etching species at low pressures and low bias, they enable the creation of layers of spherical voids at high rate. This makes it possible to fabricate a single layer of unit cells in a single etch step, which lasts a few seconds as opposed to several minutes in a conventional RIE, and in contrast to the laborious multilayer approach for the woodpile structure. In addition, this etching process should be applicable to the fabrication of photonic crystals over a range of length scales, for applications over a wide range of the electromagnetic spectrum, with little to no modification other than scaling the mask dimensions and the etch times. In the following section, I will discuss in detail the development of the three-dimensional PhC etch process.

4.1.3 Spherical Voids Etch Development

A three-dimensional simple cubic lattice can be dissected into layers of spherical voids overlapping each other. Hence, the first step in the process development is to obtain a single layer of spherical voids. An etch mask consisting of a square 2D PhC lattice designed to operate in the THz regime was used with the radius of the air holes r = 1 μm and lattice pitch a = 3μm. This approach ensured that numerous silicon samples can be fabricated using standard photolithography, a parallel process as opposed to a slow, serial e-beam lithography process. Efforts were concentrated only in the optimization of the etch process to obtain spherical voids. While a straight fluorinated etch leads to isotropic profiles, the window of the processing parameters is extremely narrow and hence necessitates laborious exploration. Hence, a robust

etching sequence is required to create a layer of spherical voids. This can be achieved by starting with the anisotropic TM-DRIE process to obtain planar PhCs such that the etch depth of the cylinder is equal to the radius of the sphere required for the fabrication of three-dimensional PhC lattice, followed by an isotropic etch, as depicted in Figure 9.

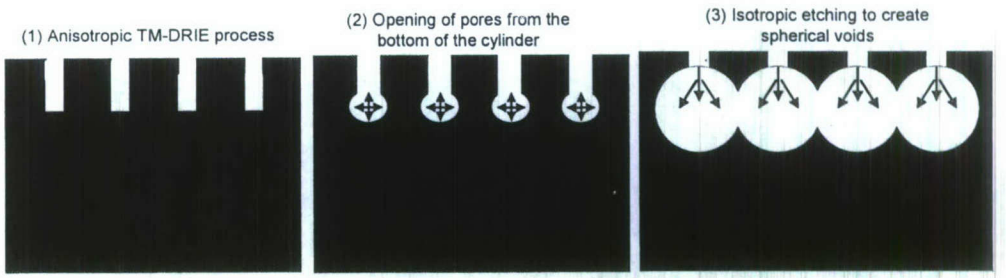


Figure 9: Schematic of the fabrication process used to obtain spherical voids.

In a perfect three-dimensional simple cubic lattice, the diameter of the spheres is equal to the lattice pitch, hence the etch depth of the cylinders is approximately 1.5 μm. This can be achieved by either controlling the TM-DRIE process in the pressure mode or in the position mode. While the pressure mode is utilized for the fabrication of planar PhCs, the etch rate/loop is 90nm. Hence to achieve an etch depth necessary for our process (1.5 μm) it would take approximately 15 minutes. However if position mode is utilized, the duration of the process would only be one minute.

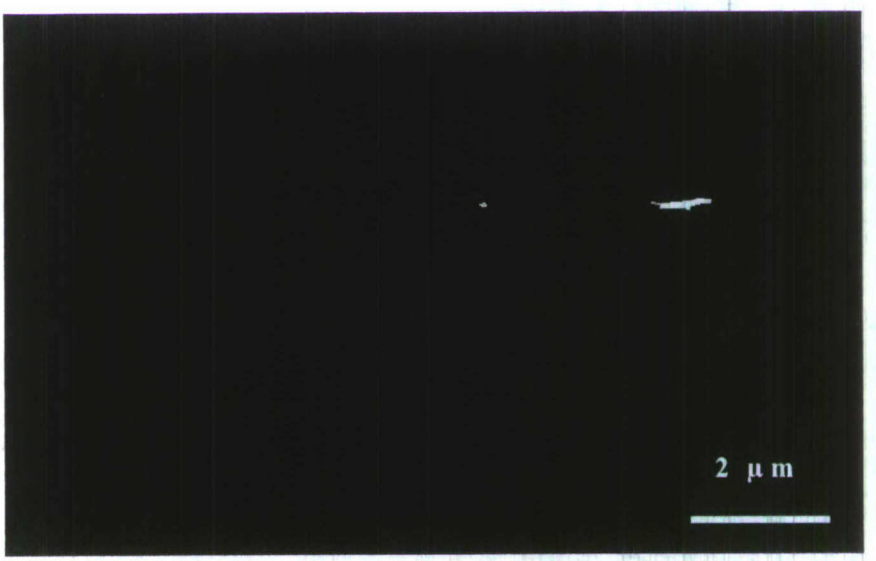


Figure 10: SEM image of a two-layer 3D photonic crystal fabricated using the proposed methodology. The first layer was over-etched, yielding voids larger than those in the second layer.

When compared to the TM-DRIE process for planar PhCs, the polymer deposition step is performed at higher gas flow rate and lower bias powers to ensure sufficient passivation. Following this step, a longer isotropic etch is performed to open the pores from the bottom of the cylinders, as the sidewall of the cylinder is protected by the passivating polymer. The pores opened at the bottom of the trenches grow and oblate eventually reaching the etch mask from below. Hence, controlling the isotropic etch times is critical in the development of spherical voids.

Once a single layer of spherical voids is obtained (single cubic unit cell), the next step is to passivate the spherical voids with a polymer and selectively open the passivation layer at the bottom of the spherical voids to create an opening for the subsequent layers. However, using this approach, only two layers of cubic unit cells could be fabricated, as shown in Figure 10.

While preliminary results of this process indicate the great potential of this method, a more robust process needs to be developed which necessitates investigation into the ability to fabricate signature etch profiles and the conformality of the passivation process.

4.1.4 Development of Signature Etch Profiles that lead to 3D Simple Cubic PhCs

Figure 11 depicts a schematic of the signature etch profiles that collectively make up the three-dimensional simple cubic lattice.

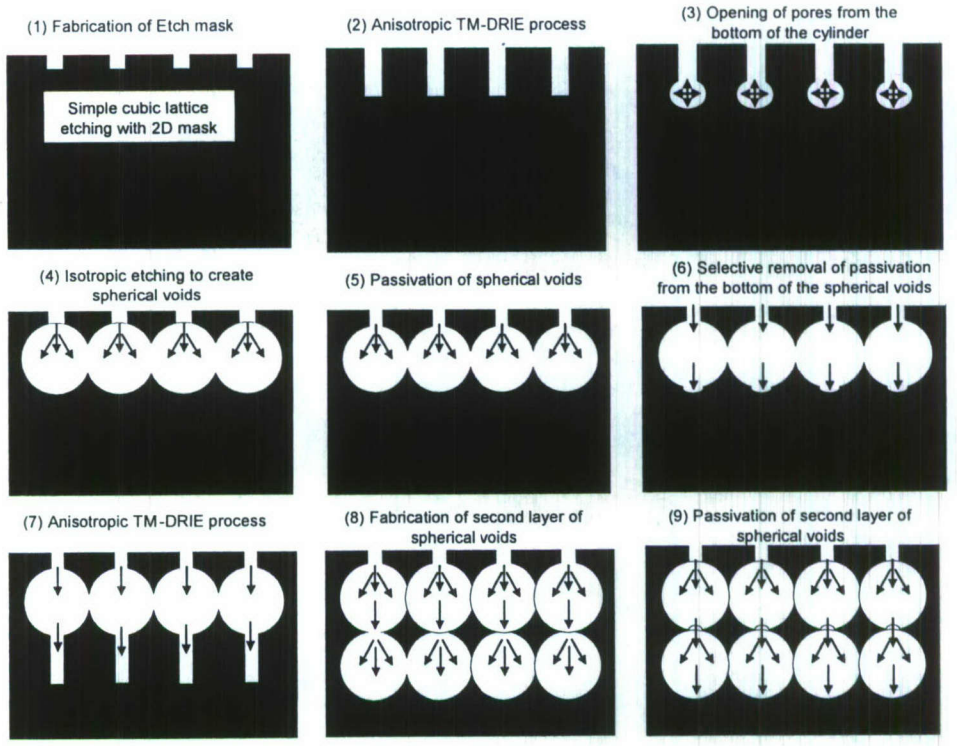


Figure 11: Schematic of the fabrication process used for the fabrication of three-dimensional PhCs. Collectively the individual signature etches make up the three-dimensional lattice.

These signature etches include creating (a) spherical voids, b) narrow trenches beneath spherical voids (lollipop structures), (c) open pores beneath high aspect ratio narrow trenches (inverted lollipop structures). In order to validate the process, one has to develop an etch "toolbox" with the above stated abilities, which is illustrated in Figure 12. These processes will be used towards realizing buried 3D PhCs in silicon.

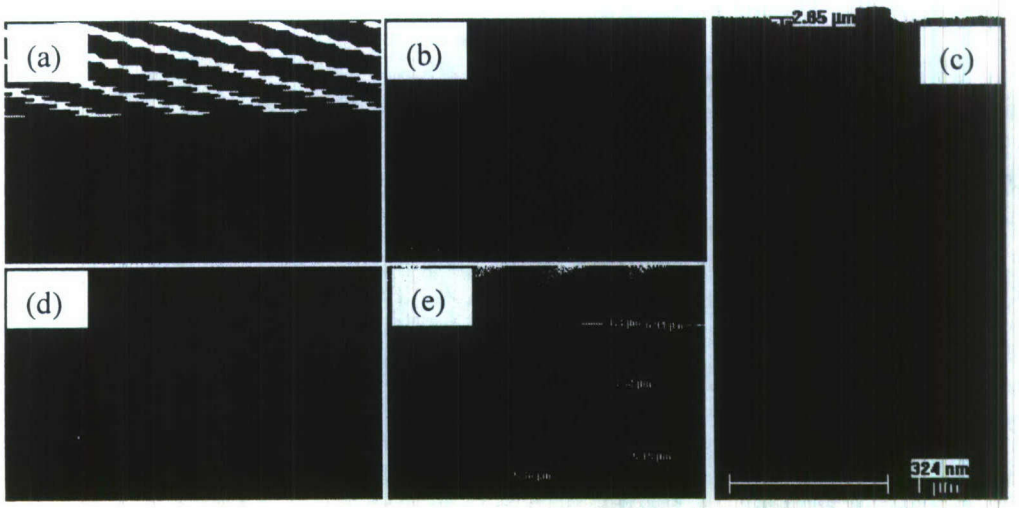


Figure 12: (a) SEM Image of a layer of spheroidal voids, (b) SEM Image of an etched deep trench with vertical profile, (c) SEM Image of a pore opened beneath a high-aspect ratio trench, (d) SEM Image an inverted lollipop structure (anisotropic etching followed by isotropic etching) and (e) SEM Image of a lollipop structure (isotropic etching followed by anisotropic etching).

Now that we have showcased the ability to create these individual signature etches, the next step involved the investigation of the polymer deposition characteristics with respect to the geometry.

It can be observed from Figure 12, that the first layer was etched longer than necessary, which resulted in non uniform void dimensions in the first and second layers. This artifact can be attributed to non-conformal passivation in the first layer of spherical voids. In order to validate this claim, I investigated the deposition characteristics of C_4F_8 with respect to the geometry of the etch profile.

4.1.5 Etch Process for 3D Simple Cubic PhCs

The wafers used in this work, consisted of 1 µm SiO_2 grown on Si using thermal oxidation techniques at SAMCO International. Prior to the fabrication sequence, the wafers were cleaned. The etch mask used in the development of low-index contrast planar PhC devices utilized e-beam evaporated Cr of few tens of nm. Hence a similar approach was followed in the development work of three-dimensional PhCs. Following 50 nm deposition of Cr using e-beam evaporation method, photolithography was performed using the designed square lattice THz photo-emulsion mask. The designed photo-emulsion mask consisted of two sets of square lattice PhCs, one with a 5µm lattice pitch and the other with a 3µm lattice pitch but both sets had constant hole diameter. Following the lithography process, the pattern is transferred into the underlying Cr layer using a wet etchant. Using Cr as the etch mask, a three step process is employed, to obtain the first layer of spherical voids,. The first step involves transferring the pattern into silicon dioxide using the TM-DRIE SiO_2 processes. The next step involves using the TM-DRIE Si process to etch a cylinder. Finally, an isotropic etch is performed to open pores to facilitate the creation of spherical voids, as depicted in Figure 13. The remaining Cr layer at the surface is stripped in a wet Cr etchant leaving behind a square PhC lattice etched in silicon dioxide and beneath it the first layer of spherical voids.

Following the creation of the first layer of spherical voids, oxidation of silicon is performed which involves heating a silicon wafer to 900° - 1300° C in atmosphere containing oxygen or

water vapor. The oxygen or water vapor (oxidant) diffuses into the silicon substrate causing an oxidation reaction. Figure 14 provides a picture of the set-up built to facilitate oxidation of spherical voids.

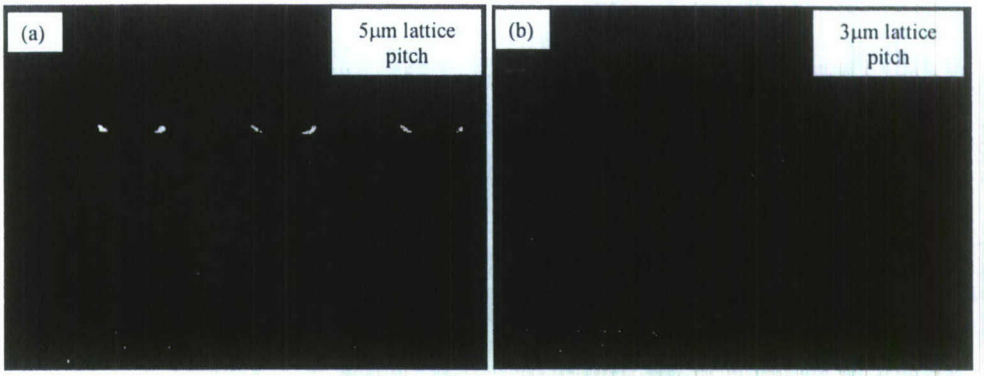


Figure 13: Cross-sectional SEM images of the first layer of spherical voids in (a) 5μm PhC lattice and (b) 3μm PhC lattice, The 5μm PhC lattice provides additional information namely; the horizontal and vertical etch depths which are useful for the process development.

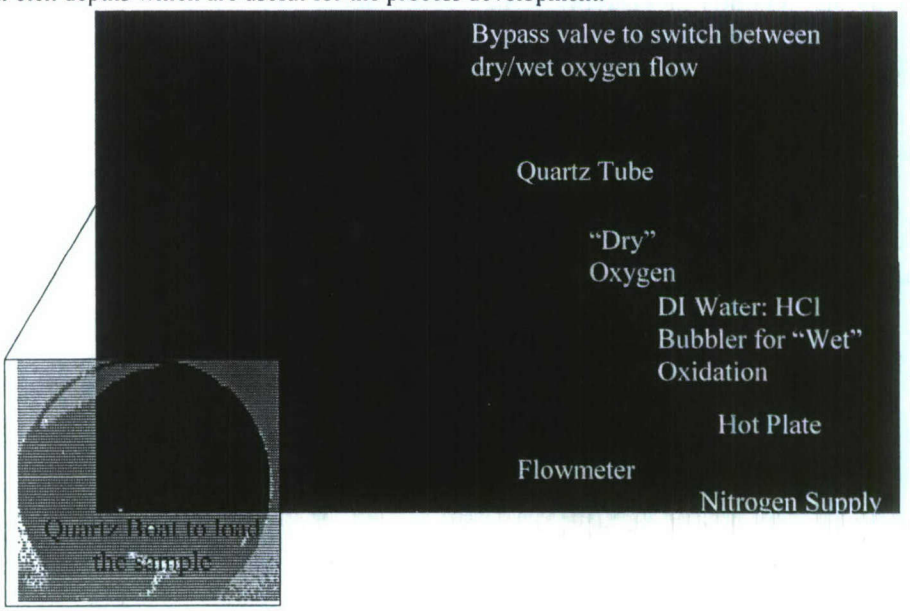


Figure 14 Oxidation set up used to passivate the spherical voids in silicon.

In our experiments, "dry" oxidation was performed at 1035° C with the oxygen flow set at 3 psi for 15 minutes. The thickness of oxide formation was measured to be around 50 nm. The next step in the process involved selective removal of the oxide from the bottom of the spherical voids. This is achieved by means of an anisotropic TM-DRIE etch process used to etch silicon dioxide. The number of cycles for which this etch is performed is extremely critical. Insufficient number of loops will leave behind a thin film of silicon dioxide which acts as an excellent barrier hence preventing any further etching or opening of pores. Excess number of loops after removing the silicon dioxide passivation layer attacks the underlying silicon due to higher bias powers in the etch process. This creates "craters" of rough etches, preventing formation of smooth spherical voids. Two loops of the TM-DRIE SiO_2 process was found to be

sufficient enough to selectively etch the oxide passivation and create an opening for the formation of subsequent spherical voids.

Having investigated the ability to fabricate spherical voids, achieve conformal passivation using silicon dioxide and selective removal of oxide passivation from the bottom of the voids, one would envision repeating these processes in a sequence to create layers of buried voids contributing to the simple cubic lattice.

However, the ability to open pores decreases dramatically with increasing depth, as can be observed from Figure 15. This is understandable because the ion density decreases at the bottom of the trench, limiting the amount of radical species available to achieve the required etch.

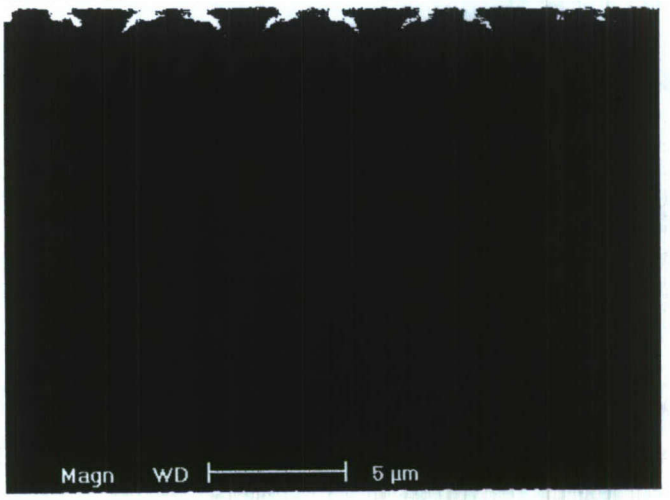


Figure 15: SEM image illustrating the difficulty to open pores and the need for scaling the etch times to achieve the required uniform diameter.

The downscaling of the pore size can be eliminated by parameter ramping, i.e. by scaling the isotropic etch times. By scaling the etch times, layers of spherical voids with uniform diameters can be fabricated, in our case the diameter required is 3 µm. After several experiments of the isotropic etches, and measuring the horizontal and vertical extent of the voids resulting from these etches, it was observed that the scaling of the etch times from one layer to another was non-linear.

4.1.6 Fabrication Results

Indeed, devices have been fabricated thus far that possess as many as six layers, as shown in Figure 16. It is important to point out that the devices fabricated thus far have lattice periods of approximately 3 µm. Such a lattice will not be expected to function as a self-guiding medium for telecommunications wavelengths. However, with our proposed 3D fabrication method, by simply reducing the dimensions of mask features and the corresponding etch times, one can readily scale down to telecomm feature sizes. Larger mask dimensions have been used thus far simply for convenience, since such masks are more easily and rapidly fabricated by i-line UV photolithography, whereas telecomm masks require more tedious or less mature techniques such as e-beam lithography or UV interference lithography.

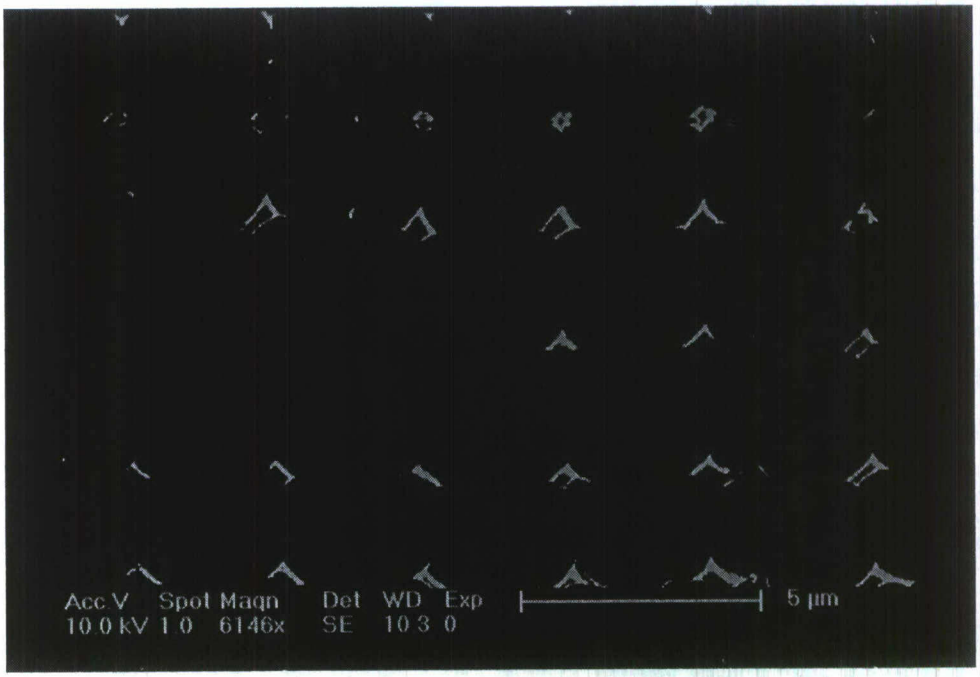


Figure 16: SEM image of a six-layer cubic unit cell fabricated using scaling of the isotropic etch times. Table 5.4 provides the process parameters used to fabricate this structure.

4.1.7 Experimental Characterization Results

Out-of-plane spectral characterization measurements were performed to confirm the device characteristics that would be expected from the fabrication of a high-index-contrast six-layer cubic unit cell. In particular, the spectral location and strength of directional stop bands were probed at varying incident angles in the reflection mode. Reflection measurements were obtained using Fourier Transform Infrared Spectrometry. The fabricated 6-Layer simple cubic three-dimensional PhC shows a reflectivity of 100% !+, as shown in Figure 17 which implies the strong presence of stop bands in the 6.2 - 9 µm range and possible band gap characteristics.

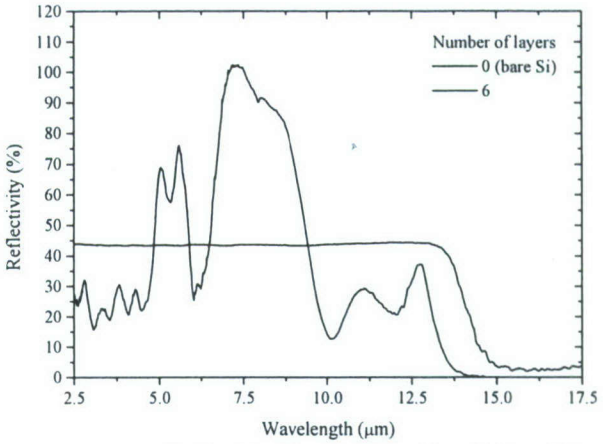


Figure 17: Reflection measurements obtained by Fourier Transform Infrared Spectrometry. One can observe high reflectivity, indicating presence of stop bands in the 6.2-9 μm range.

While this result is extremely promising for filtering or other PBG-based applications, our goal is to leverage artificial structuring of silicon to realize chip-scale optical interconnects based on the self-collimation phenomena discussed earlier for which the equi-frequency contours should be square-like. From the SEM image of the six-layer cubic unit cell, depicted in Figure 18 (a), the lattice constants in the horizontal and vertical direction were calculated and averaged. These values were adopted to perform electromagnetic simulations to investigate the presence of a square-like equi-frequency contour. The results are summarized in Figure 18(b). At a normalized frequency of 0.51 c/a, we can observe a square-like EFC, indicating that the fabricated structure can be used to confine and guide light in three-dimensions without any structural waveguide-confinement" mechanisms.

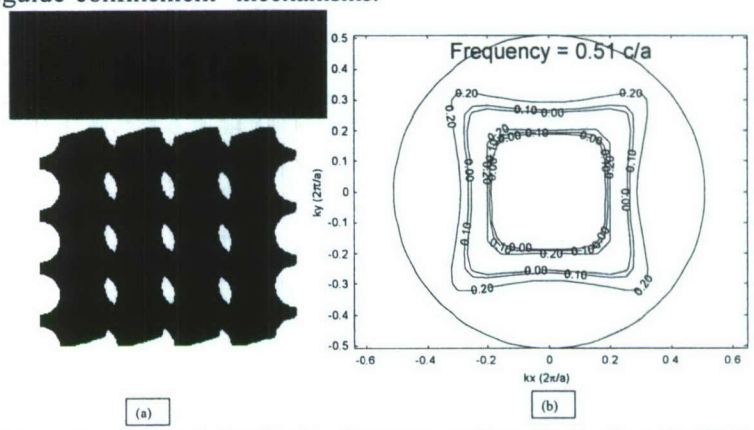


Figure 18: (a) Computer rendered visualization for an approximately simple cubic PhC structure, whose dimensions are provided in the inset in the figure. Note: These measurements were obtained from the actual sample. (b) Electromagnetic simulations indicating the presence of a square-like EFC, which proves to be extremely useful in confining and guiding light in three dimensions without any "waveguide confinement" mechanisms. The figure shows the EFC at different k_z.

4.2 Photonic Crystal Based Analog to Digital Converter

Dr. Antonio Crespo expressed interest in collaborating to design and implement a photonic crystal "analog to digital converter" (ADC), shown in Fig. 19. In this application, he proposed the use of a cascading array of beam splitters and detectors, to split the power of an

incoming optical signal into multiple channels, by a specific percentage that correspond to a specific digital representation of the signal.

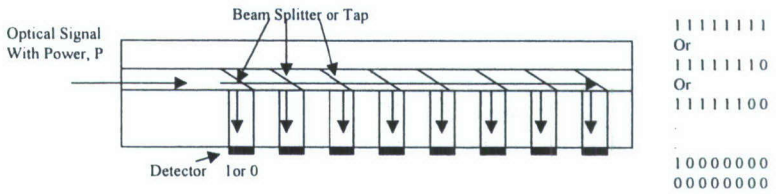


Figure 19 Analog to Digital Converter

Here, a strong signal will have enough energy for detection along the entire waveguide path. As the signal strength is reduced, the power progressively becomes too weak for detection at the most distant detectors. Thus, the digital representation follows the characteristics shown on the right of Figure 19 from the maximum to minimum power level.

Based on concept design provided by Dr Crespo, it was the role of our researchers to determine the appropriate Photonic Crsystal based design which accounts for precise splitting ratios of the various beam splitters. An example of a 2 bit ADC is shown in Fig. 20. The number of beam splitters used is 3 which will produce 4 different states.

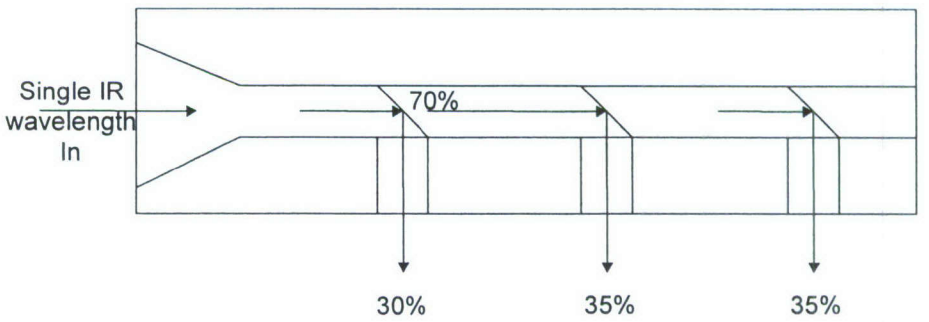


Figure 20 A 2 bit ADC concept design using 3 beam splitters

- **Challenges**

1. Precise control over the various splitter ratios.
2. Minimize delay due to unequal optical path length
3. The design should account for fabrication tolerances and its impact on splitter ratios

4.2.1 High Resolution ADC using self-collimated PhC Waevgiudes

- We examined another design for an ADC relying on engineering the dispersive properties of Photonic Crystals instead of their confinement properties. The design combines a self collimation photonic crystal structure with a mirror structure constructing the elements of the beam splitters.
- By engineering the transmission/reflection properties of the mirrors structure high precision splitting ratios can be achieved and hence high resolution ADC designs can be implemented
- The hybrid structure created was called a variable beam splitter, and is shown in Fig. 21

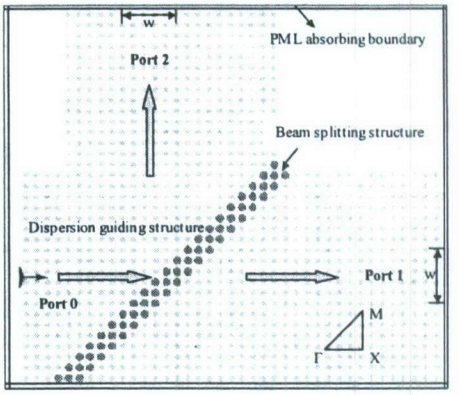


Figure 21 Dispersion based tunable beam splitter utilizing a hybrid PhC structure

- Controlling the design parameters of the beam splitting structure (mirror) controls the splitting ratio.
- Shown in Fig. 22 are the steady state results obtained by running a numerical experiment on the structure shown in Fig.21 Shown in the figure are three different cases with different splitting ratios

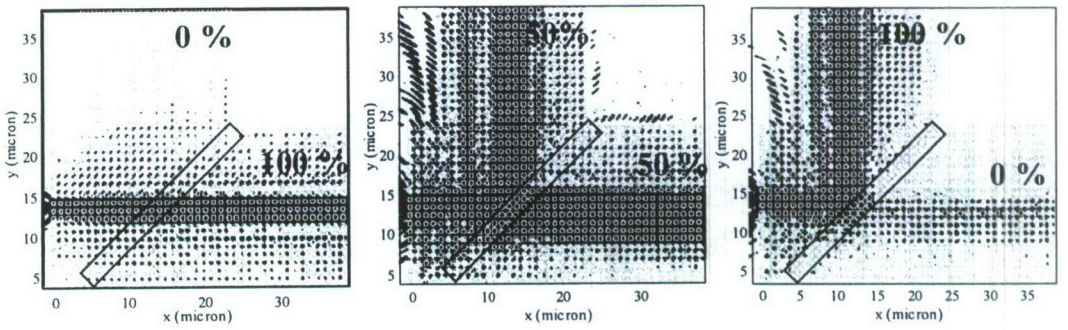


Figure 22 Three-steady state snapshots of the structure shown in Fig. 21 with various split ratios between port 1 and port 2

4.2.2 Prototype Fabrication

The three common PBG fabrication processes based on silicon on insulator (SOI) methods are electron beam lithography (EBL), interferometry, and self-assembly techniques. we concentrated on EBL on SOI technology as it is based on the well-established methods of the semiconductor industry and offers the best potential for small feature sizes and large volume production. SOI is an attractive platform for realizing dielectric waveguides and photonic band gap devices due to the large refractive index contrast between the silicon waveguide and the underlying SiO_2 layer. The refractive index contrast is necessary to confine light in the plane of the photonic crystal lattice and to realize a photonic band gap for lateral confinement in the waveguides. In Phase I, we fabricated devices that follow the processing steps shown in Figure 23.

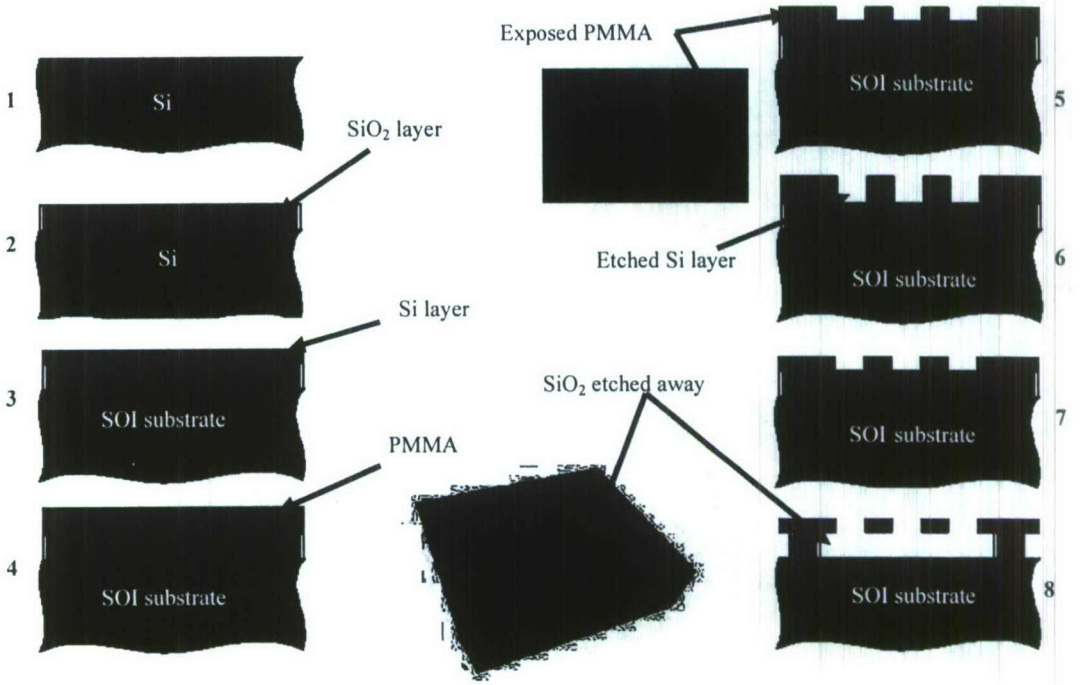


Figure 23. Silicon On Insulator Fabrication Process.

In this process a SiO_2 layer is deposited on a blank silicon wafer. Next, a layer of silicon is bonded to the SiO_2. PMMA is spun on the substrate and is used as an electron sensitive resist. Utilizing the unparalleled resolution of electron beam (e-beam) lithography, the PMMA is exposed and developed. Reactive Ion Etching (RIE) is then used to transfer the pattern to the silicon layer. In this step, it is important that the cylindrical structures that make up the PBG are etched with a high degree on anisotropy. To this end, the University of Delaware has developed a Bosch-like etching process that produces devices with straight walls and high aspect ratios. This process consists of a three step etching cycle, which is repeated a number of times to achieve the desired etch depth. First, a sidewall passivating polymer film is deposited using CF_4 and H_2 gases. The deposition is followed by two etch steps that use a mixture of SF_6 and He gases. The passivating film prevents the Si sidewalls from being isotropically etched by the SF_6 discharge, which contains a large concentration of atomic Fluorine. During the subsequent etch step, 'the smash,' the passivating polymer film is preferentially removed from the bottom of the trenches due to hard ion bombardment in a SF_6 and He plasma. In the second etching step, the SF_6 and He plasma, containing a large concentration of atomic Fluorine, etches the silicon in the preferred downward direction, while the passivating polymer prevents sidewall etching. The experimental variables that were optimized to arrive at the custom etch recipe included RF power, etch time, smash time, gas composition, etch pressure, deposition time, gas flow rates, and chamber conditions. This custom technique provides high selectivity, largely vertical sidewalls, and repeatability. Following the RIE step, SiO2 layer below the silicon PBG is etched away.

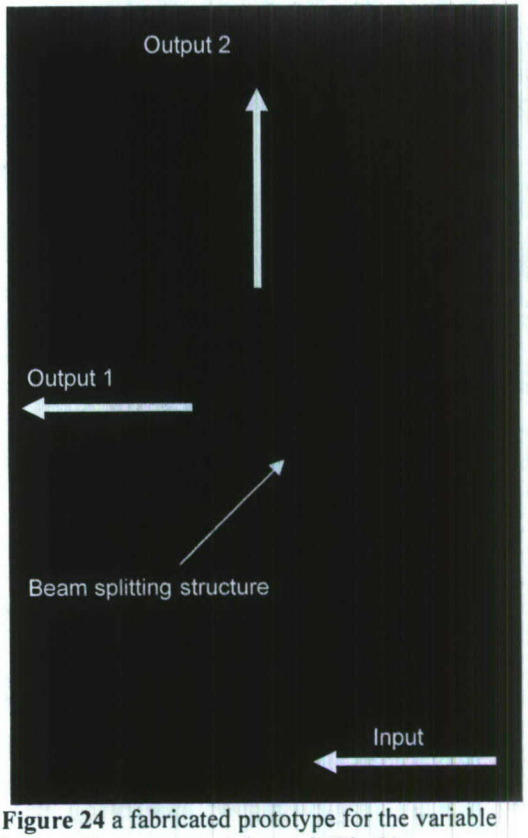


Figure 24 a fabricated prototype for the variable beam splitter structure shown in Fig 21

In Figure 24, we show the fabrication results for dispersion based variable beam splitter combing both a PBG and PhC structures. A J coupler is fabricated at the input and the output ports of the structure to facilitate efficient coupling form a conventional dielectric waveguide to the PhC structure.

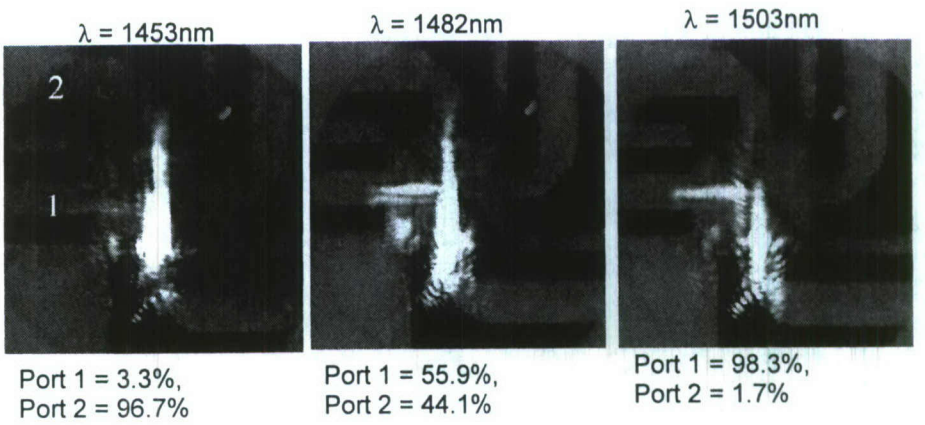


Figure 25 experimental validation for the variable beam splitter structure shown in Fig 24

Preliminary testing of the device is shown in Fig. 25, which is shown to be in agreement with our previously presented numerical results shown in Fig. 22, where we were able to experimentally validate the three cases presented numerically.

4.2.3 Two-Bit A/D implementation

Our first approach toward implementing a photonic crystal based optical analog to digital converter is to combine a self-collimated photonic crystal waveguide structure with an array of splitters formed by etching a small slit. Varying the slit width controls the ratio of the transmitted/reflected beam through the various branches as shown in Fig. 26

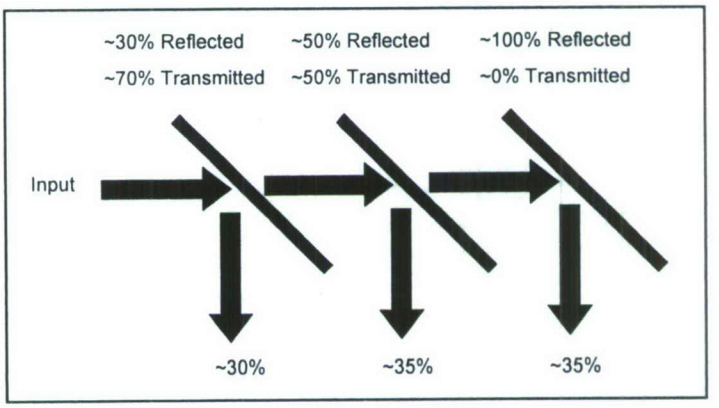


Figure 26 Specification received for a two bit A/D

Prior to exciting the structure with a monochromatic light wave at the input port, careful study of the relationship between slit width and splitting ratio was performed to determine the appropriate slit dimension to provide the performance expected of each branch.. In an absence of a slit structure an incident light beam incident through the input port will be self-collimated through the photonic crystal structure and will exit at the output port I with no distortion. Once a slit structure is introduced, it will interact with the incident light beam through the input port as to divert part of the incident beam toward output port II and allow the other part to exit at port I. the width of the slit structure determines the proportion of the light exiting at port I versus that

exiting at port II. If the slit structure is wide enough, it will act as a reflecting mirror in which case, the incident light will completely diverted to port II. We identified this to be a threshold value of the slit structure and referred to it as $W_{threshold}$. Hence any slit width equal to of greater than $W_{threshold}$ will completely reflect the incident light to exit at port II. While for values of ($0 < W_{Slit} < W_{threshold}$) partial splitting will occur.

4.2.4 Experimental Demonstration of a Two-Bit A/D

To experimentally validate the design concepts of the 2-bit optical A/D converter, we first fabricated the self-guiding lattice on a silicon-on-insulation (SOI) wafer, which has 260nm-thick silicon device layer on a 1μm-thick SiO_2 insulating layer. E-beam lithography and inductively coupled plasma (ICP) dry etching was employed to pattern and transfer the structure to the silicon device layer. The underneath SiO_2 layer was removed using buffered oxide etching (BOE). Figure 27 shows SEM micrographs of fabricated splitters. The self-guiding region of splitters consists of a square array of air holes. The radius of air holes is 220 *nm* and the lattice constant *a* is 450 *nm*. The splitters are diagonal rows of air holes with different radius from self-guiding region. To test these fabricated splitters, the sample was cleaved and light from tunable laser was coupled onto the input facet of a tapered dielectric waveguide by a tapered polarization maintained fiber. The tapered waveguide is interfaced with the self-guiding lattice along the Γ-X1 direction. When the wide beam from fiber is narrowed down by the tapered waveguide, it is self-collimated and guided by the PhC lattice along the Γ-X2 direction.

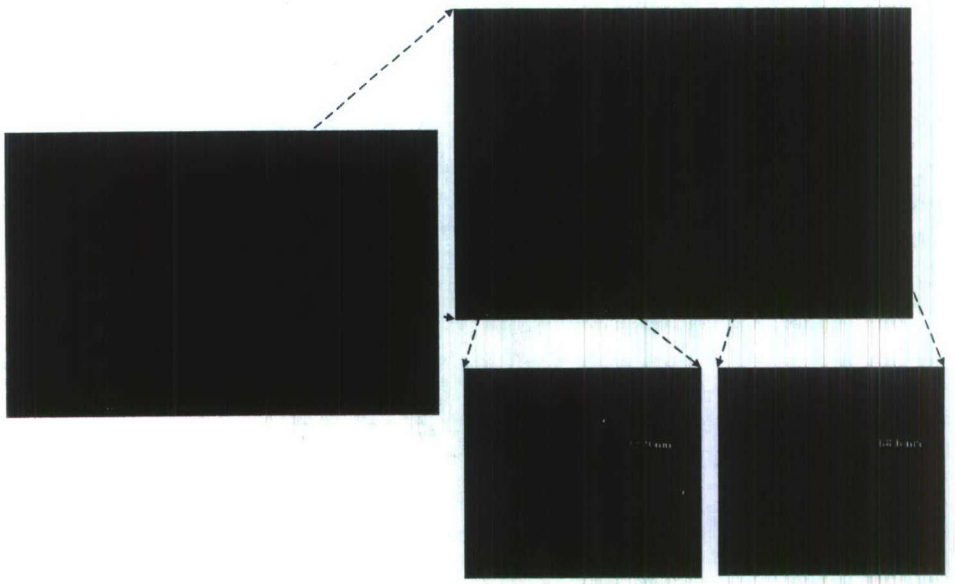


Figure 27 A Fabricated Two bit A/D prototype

A narrow self-guiding beam is beneficial to high-density integration. When the self-guiding beam propagates through the uniform lattice and arrives at the splitting structure, it splits between a transmitted light and the reflected light. The splitting ratio varies with the size of air holes of the splitting structure. Figure **28** demonstrates this behavior, where (a) is the top-down images captured by an IR CCD camera for the case with the radius of the splitting structure of 368 nm at the wavelength of 1560 nm. In contrary to the normally observed enlightened light guiding path in the case of PhC band gap line defect waveguide, the self-guiding path is absent of any observable light, which indicates low radiation loss due to the fact that the selected mode region falls outside the light cone as illustrated above.

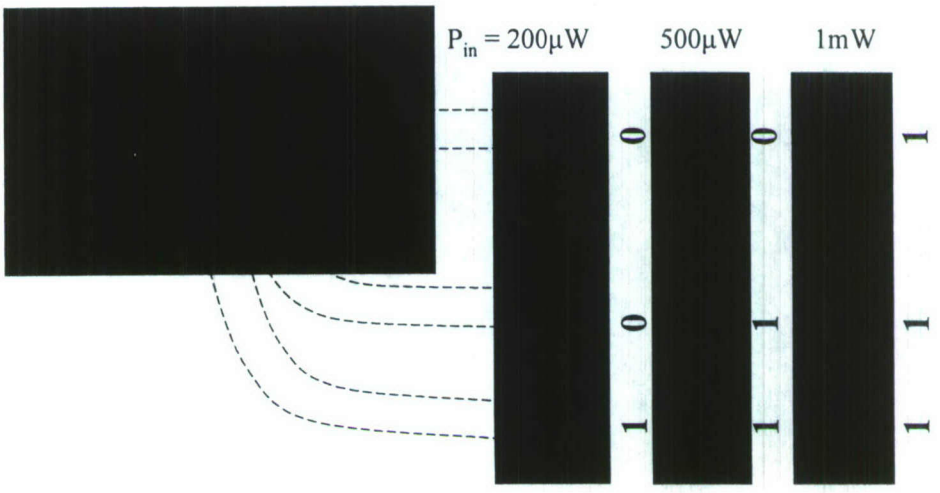


Figure 28 Experimental Characterization of the two bit A/D shown in Fig 27

However, due to the break up of the lattice uniformity, the perturbed splitting air holes cause some radiation loss). On the other hand, the fact that only a narrow part of the splitting structure is enlightened shows that the propagating beam is well confined laterally by the self-guiding lattice. The large bright spot at the left hand side is the scattered light at the intersection between the dielectric waveguide and the self-guiding PhC lattice, which might be caused by the discontinuity of the effective index between two materials and could be improved using adiabatic structure.

4.3 Photonic Crystal Based Multi-Spectral Receiver

During the effort of this project, Dr. Soref proposed a "Multi-Spectral Receiver" (MSR) shown in Figure 29,

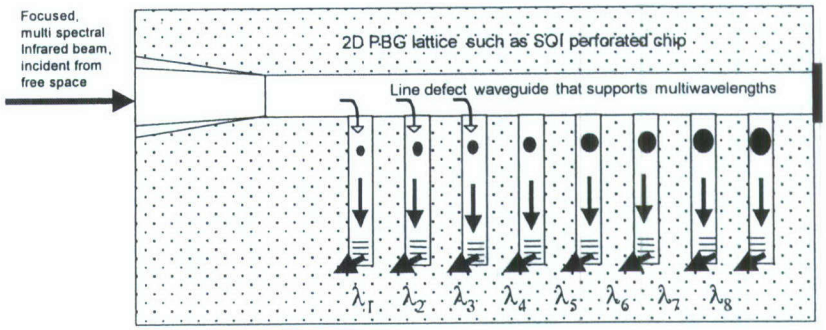


Figure 29. A multi-Spectral Receiver

In this application, a multi-spectral infrared beam is launched in a PBG waveguide that supports the wavelengths of interest. Resonators are used for filtering individual wavelengths into separate guides. The entire silicon wafer is bonded to a detector array, thereby monitoring each wavelength independently. Dr. Soref mentioned that a suitable detector array is also under development at AFRL.

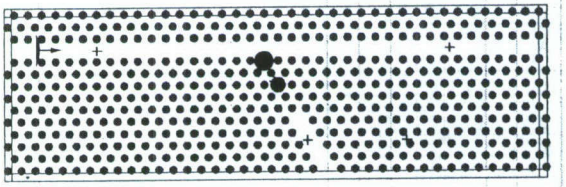


Figure 30. Wavelength Tap, Graphical Model.

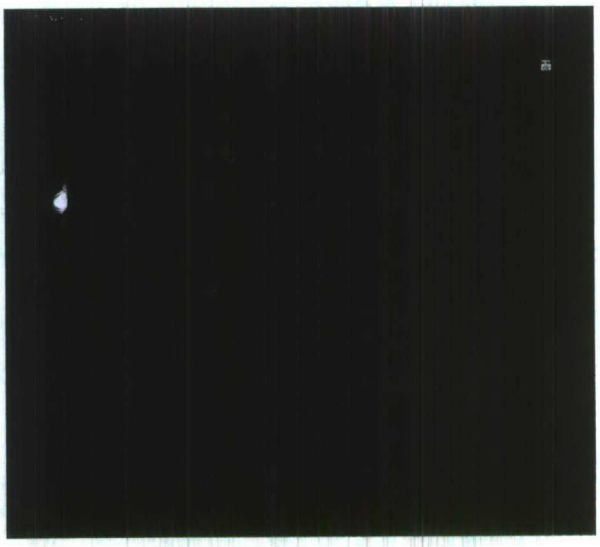


Figure 31 EMPLab Simulation

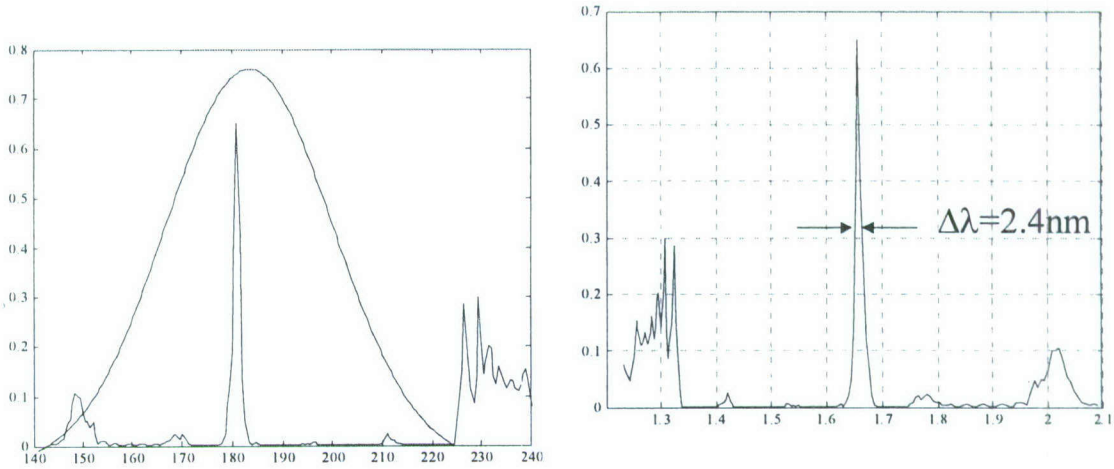


Figure 32. EMPLab Results, a 2.4nm filter

As previously described, the Multi-Spectral Receiver is based on a PBG waveguide that supports the wavelengths of interest. Resonators are used for filtering individual wavelengths into separate guides. In Figure 30, a silicon and air hole lattice is represented with a multi-spectral source (red arrow graphic) and a defect resonator for wavelength selection.

Our analysis shows that over very large wavelength bands, filter taps can be fabricated that allow for better than 2.5 nm resolution which is appropriate for the MSR application.

In Figures 33 and 34, we show the fabrication results for the MSR system. A primary waveguide was fabricated that supports multiple wavelengths. Defects of various sizes were produced to measure wavelength filtering.

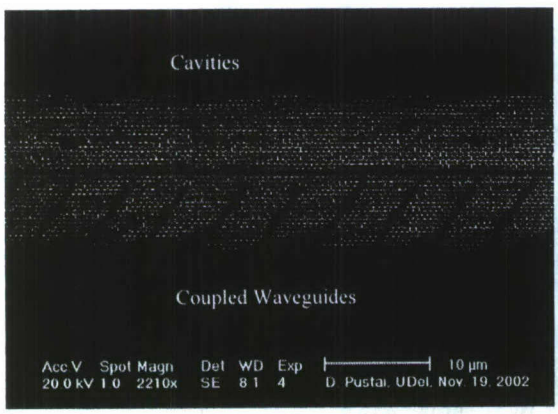


Figure 33. Defect -Tuned Channel Drops

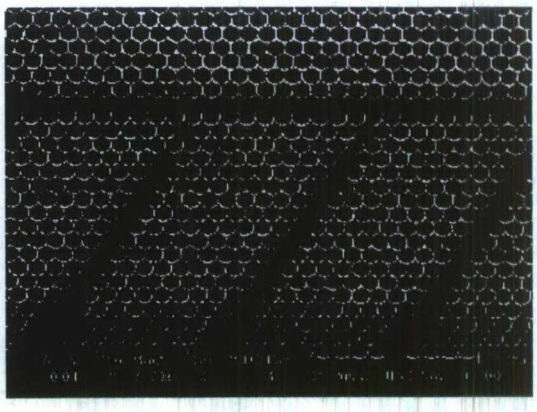


Figure 34. Defect -Tuned Channel Drops

Preliminary testing of this device indicated that due to tight tolerances, defects may have to be larger to achieve sufficient coupling into the tapped guides. Hence even though using point defect approach is ideal for attaining narrow band filtering, it is highly sensitive to fabrication tolerances which has to be within or less than 5%. Hence in search for another alternative which may not require as high fabrication tolerances, we collaborated with Dr Soref and came up with the structure shown in Fig. 35

The simulation and experimental results presented in Part I of this report can be further utilized to implement a static or a dynamic Multiple Spectral Receiver by examining the

frequency response of each splitter or of an array of splitters over a wide frequency range. Such behavior can be further engineered to provide filtering as shown in Fig.35 below.

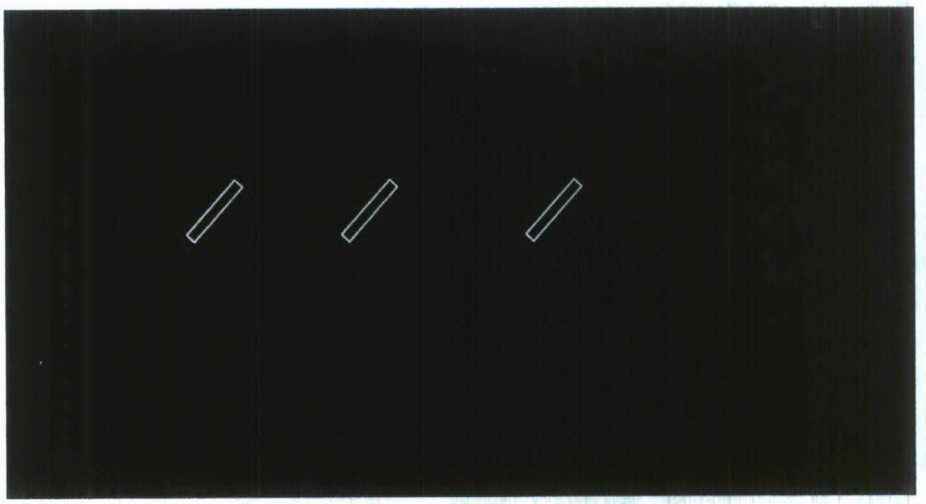


Figure 35 Utilizing the A/D design in part I to perform as a wide band frequency selective filter

Consider the structure consisting of 3 splitters shown in Fig.36 if a broadband pulse is incident through the input channel, each splitter will respond to the various frequency content of the incident signal differently and hence temporal filtering can be attained, as shown in the experimental results shown in Fig. 37

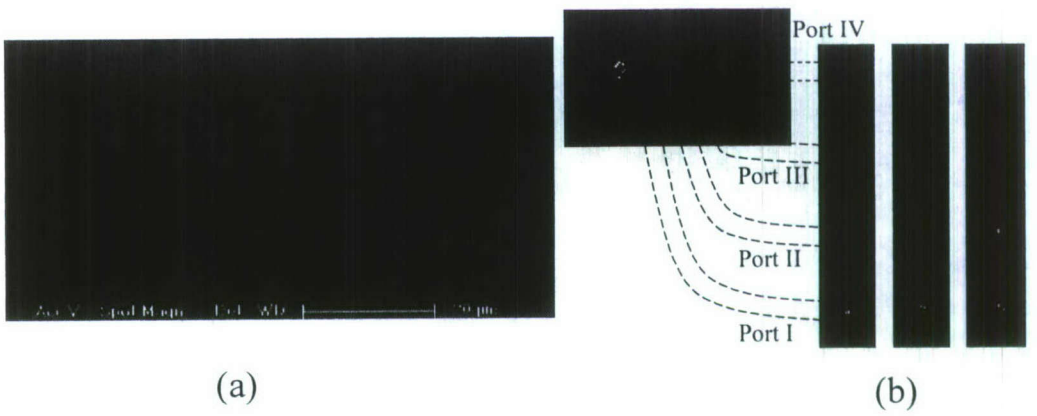


Figure 36 A 3 splitter A/D structure

From the results shown in Fig 36 we can see that by careful design and engineering of the properties of the various PBG splitter layer one can implement frequency selective filtering

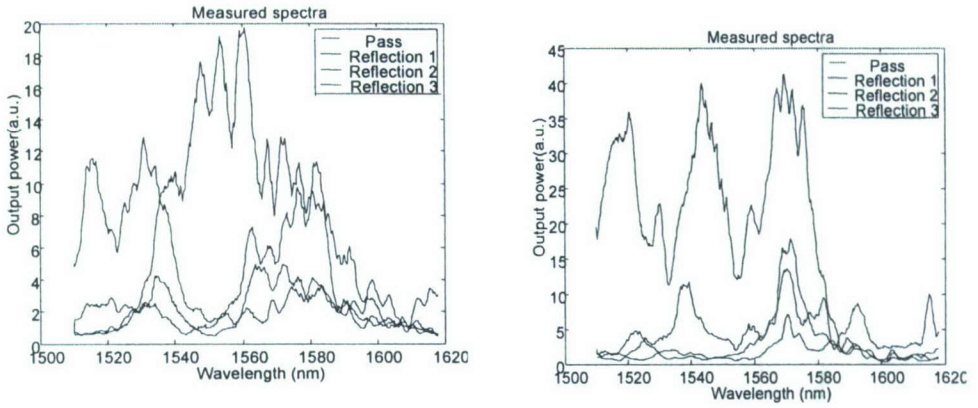


Figure 37 Transmission spectra measured experimentally for two different prototypes containing 3 splitters each

If the static splitters shown in Fig. 35 were to be replaced with PN or PIN junctions to create active splitters, additional more exciting functionalities can be further integrated within our A/D-MSR Photonic crystal based device. Additional functionalities include 2 by 4 and 4 by 4 optical switching. In addition the number of splitters necessary to implement an N-bit will be linearly proportional to the number of bits; i.e., 3 splitters will only be needed to implement 3 bit A/D instead of 8 splitters as in case of the static implementations. Also a reconfigurable switching fabric can be also implemented.

4.4 *Tunable Open Resonator*

Recently, a self-collimation-based open resonator was demonstrated in photonic crystal structures where a vertical coupling mechanism was used to efficiently excite the self-collimated beam by placing a dielectric waveguide above the self-collimation lattice. Using EMPLab^{TM} implemented on a graphical processing unit (GPU) we designed a small propagating wave cavity shown as the inset of Figure 38. In this design, we used an in-plane air slit to couple light out to of a dielectric waveguide. The output spectrum is shown as a blue solid line in Figure 39, and demonstrates that the desired resonant property of a cavity has been achieved. The little second peak to the left of each resonant peak is caused by the mismatch between the excitation of a Gaussian beam inside the lattice and the self-collimation mode. Varying the background refractive index by 1e-3 results in a completely shifted output spectrum shown as the red dash line in Figure 39. Light intensities measured at the outputs at the wavelength of 1.5851 μm are 0.1405 and 0.0025, respectively. This implies that we can switch the light on and off with an extinction ratio of 17.5 dB when the refractive index is changed by merely 0.001.

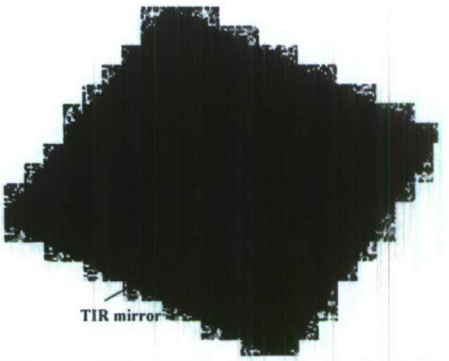


Figure 38. Self-collimation photonic crystal open resonator.

4.5 Si-based EO-SCPhC Modulator

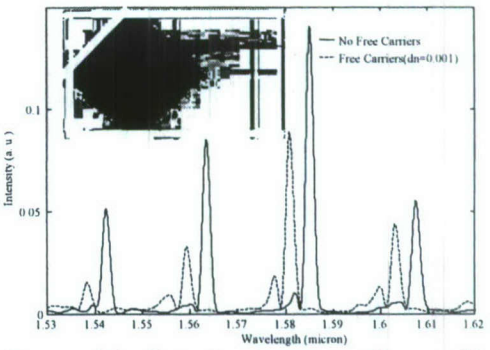


Figure 39 Output spectrum of a self-collimation photonic crystal propagating wave cavity.

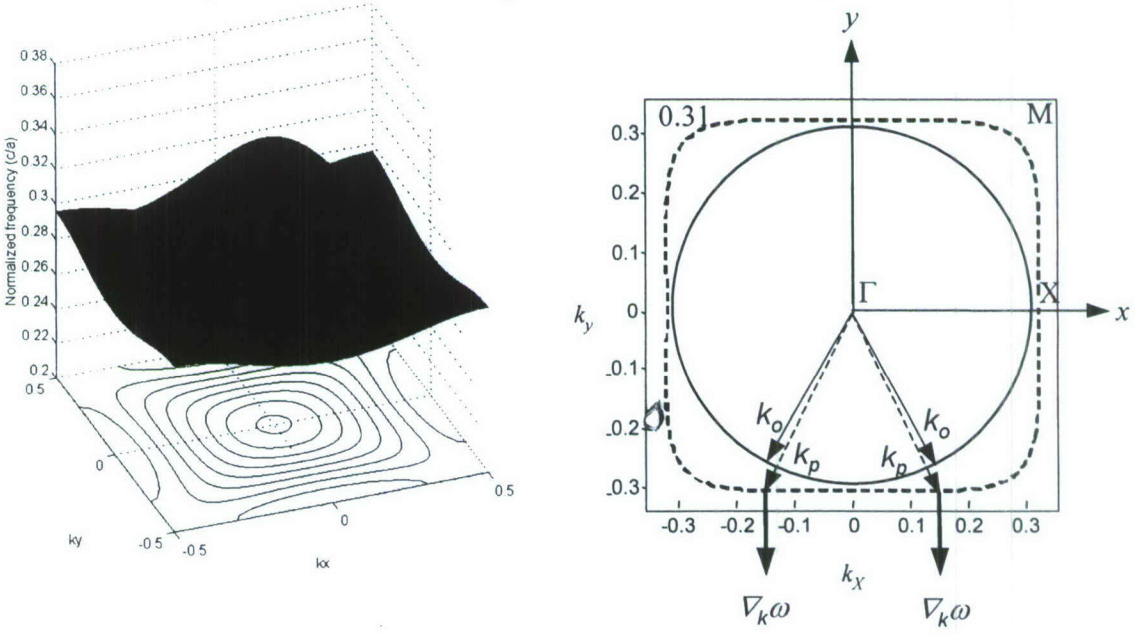
In order to build all-optical computing units, as well as practical high-bandwidth all-optical wavelength converters and modulators, we need to be able to modulate light externally in a chip-scale, highly integrated platform. The ability to pattern nanoscale structures at wafer scales, the existence of commercial electronic chip fabrication foundries, and the low optical loss and high mode confinement available in silicon waveguides all combine to male silicon-on-insulator an attractive material system for very-large scale integrated photonics.

Materials that incorporate periodic variations in constituent parameters, e.g., conductivity, permittivity, and permeability, are often referred to as photonic or electromagnetic crystals. As such, they exhibit a frequency dependent behavior as the wavelength of an electromagnetic wave within the material approaches the periodicity of the parameters, in much the same way as an electron interacts with an atomic lattice as its deBroglie wavelength approaches the atomic lattice constant. For this reason, the nomenclature for describing and representing the interactions of waves in a photonic crystal (PhC) are derived from the field of solid-state and semiconductor physics. As is well known, the behavior an electron in a solid-state material is best represented by its corresponding dispersion diagram, which provides a relationship between the electron energy (and indirectly its deBroglie wavelength) and its direction of transport within the crystal lattice. In a directly analogous fashion PhCs are represented in a similar way where an electromagnetic wave interacts with a "scattering" center that is placed on a periodic grid (analogous to the electrostatic scattering of atoms in a lattice). In this case, when the wavelength is large compared to the periodicity of the PhC lattice the wave sees it in a collective sense, wherein the periodic parameters take on an "effective property." In this case the wave takes on isotropic propagation properties and therefore follows the "light line" propagation characteristics of free space. However, as the wavelength approaches the periodicity of the lattice, collective scattering begins to significantly influence wave propagation. In addition, depending on the spatial arrangement and geometrical form of these parameters this behavior may be spatially dependent. In some cases, certain frequencies are actually forbidden within the material, in which case one has a band gap. In other cases, one may have certain frequencies that are forbidden only in certain directions within the material, which is referred to as a stop-band. It is also possible to influence the propagation of a wave without the presence of a band gap, in which case the curvature of the band structure serves to control wave propagation. Types of dispersion control include: slowing of the group velocity, super prismatic dispersion, self-collimation, negative refraction, frequency scaling through acoustic interactions, and left handedness. While each of these characteristics stem from a different type of interaction within an engineered material, all of them are clearly represented in the materials electromagnetic dispersion profile, or band structure.

Applications relying on the dispersive properties of photonic crystals have recently attracted the attention of the wide majority within the photonic crystal community. The reason for such is the flexibility of implementing similar functionalities offered by the confinement properties if operating in the stop or bandgap but yet without the limitation of high fabrication tolerances [1], alignment required or the need for high index contrast between the materials used to construct a PhC structure. Such requirements have greatly hindered the physical implementation of photonic bandgap based devices outside research laboratories and to only small device areas. It is highly believed that engineering the dispersion properties of photonic crystals will truly open new frontiers towards their true introduction to the commercial market without the need for tight

fabrication tolerances or high index materials to open a bandgap for confinement based applications. It is also believed that current replication methods can be utilized towards implementing photonic crystal dispersion based devices over a large area and hence overcoming slow fabrication throughput of fabricating a single operative device.

Light propagation through a photonic crystal structure is governed by its dispersion surfaces. Incident light waves propagate in directions normal to the dispersion surface, as shown in Figure 40. Curvature of the dispersion surface, as shown in Figure 40(a), can indicate beam divergence or convergence, whereas the lack of curvature, or straight EFC contour lines, leads to the so-called self-collimation phenomenon, as shown in Figure 40(b). Self-collimation—also known as auto-collimation or self-guiding—allows a narrow beam to propagate in the photonic crystal without any significant broadening or change in the beam profile, and without relying on a bandgap or engineered defects, such as waveguides. This property can be used for waveguiding and dense routing of optical signals. Tailoring the dispersion characteristics of a photonic crystal structure to create unique devices has been an important area of research[2, 3].



(a) (b)

Figure 40 - The dispersion surface for a PhC comprised of a silicon slab patterned with air holes, designed to have a square EFC for specified frequencies. (a) A dispersion surface. (b) A square EFC. k0 is the incident wavevector, k is the wavevector in the PhC, and $\nabla k\omega$ is the group velocity in the PhC corresponding to wavevector k. The circular EFC, corresponding to the same frequency in an unpatterned slab, is included for comparison.

To understand self-collimation, consider a planar PhC consisting of a periodic array of cylindrical air holes embedded in a high-index slab. In this case, an electromagnetic wave propagating within the plane of the periodic structure interacts with it in both the vertical and lateral directions. In the vertical direction, we only consider field configurations that are confined to the slab by total internal reflection, i.e., those that lie below the light line [4] . On the other hand, in the lateral directions, the interaction is most appropriately interpreted through a dispersion surface, which characterizes the relationship between the frequency of the wave, ω, and its associated wavevector, **k**. Dispersion surfaces can be obtained by casting Maxwell's equations into an eigenvalue problem, which can be solved using various computational-electromagnetic techniques, such as the plane-wave method [5](PWM) or the finite-difference

time-domain (FDTD) method [6]. The set of solutions, takes the form of a dispersion surface, as shown in Figure 40(a). To obtain such a rendering, one simply computes the eigenfrequencies for wavevectors at all *k*-points *within* the irreducible Brillouin zone, and then exploits the appropriate symmetry operations to obtain the entire surface shown in Figure 40(a).

In general, the dispersion surfaces, obtained by primarily employing the PWM, correspond to index ellipsoids in conventional crystalline optics, where the length from the surface to the Γ-point ($k_x = 0$, $k_y = 0$) is related to the refractive index. In the case of PhCs, however, the dispersion surfaces can take a variety of shapes depending on the lattice type, pitch, fill-factor, or index of refraction of the constituent materials, in addition to the strictly ellipsoidal surfaces of conventional materials. At the same time, we are particularly interested in the EFCs, as they characterize the relationship between all allowed wavevectors in the structure and their corresponding frequencies. For example, while the EFCs of an unpatterned homogeneous silicon slab are circular as depicted by the solid line in Figure 40(b), the EFCs of a silicon slab with periodic patterns can exhibit a variety of shapes [7]; by carefully selecting the frequency, one can obtain the square shape EFC shown by the dashed contour in Figure 40(b).

The ability to shape the EFCs, and thereby engineer the dispersion properties of the PhC, opens up a new paradigm for the design and function of optical devices. The importance of the EFC shape stems from the relation

$$\mathbf{v}_g = \nabla_k \omega(\mathbf{k}) \quad , \tag{1}$$

which says that the group velocity, v_g, or the direction of light propagation, coincides with the direction of the steepest ascent of the dispersion surface and is perpendicular to the EFC, as indicated in Figure 40(b). In the case of a circular contour, an effective refractive index can be calculated from the radius of the EFC following Snell's law. However, for self-collimation, we desire a square EFC, in which case the wave is only allowed to propagate along directions normal to the sides of the square. As a result, it is possible to vary the incident wavevector over a wide range of angles and yet maintain a narrow range of propagating angles within the PhC.

As with defect-based devices, confinement to the slab is governed by the TIR condition imposed at the core/cladding interface. However, since we are expanding the dispersion diagram by calculating the full dispersion surface in order to obtain the EFCs, we must likewise expand the light line to a light cone as shown in Figure 41. In this case, if the entire EFC is at a frequency below the light cone, light will remain confined to the slab. In Figure 42 (a) we plot the dispersion surface and light cone for the second (conduction) band and find that they intersect around an approximate normalized frequency of $a/\lambda = 0.31$, where a is the PhC lattice constant and λ is the free space design wavelength. Therefore, above this normalized frequency light would not remain confined to the slab and couple to the air mode. However, if we operate in the first (valence) band of the PhC, we observe from Figure 42 (c) that the entire dispersion surface for this band lies entirely below the light cone. Therefore, when operating in the valence band, the light remains confined to the slab regardless of its frequency, and thus, it is obviously preferable to design a PhC to achieve self-collimation in the first band.

However, while feasible, such structures are more difficult to realize for optical wavelengths because the PhC lattice constant a and hole radius r are much smaller. Therefore, a majority of the devices presented here operates in the conduction band of the PhC.

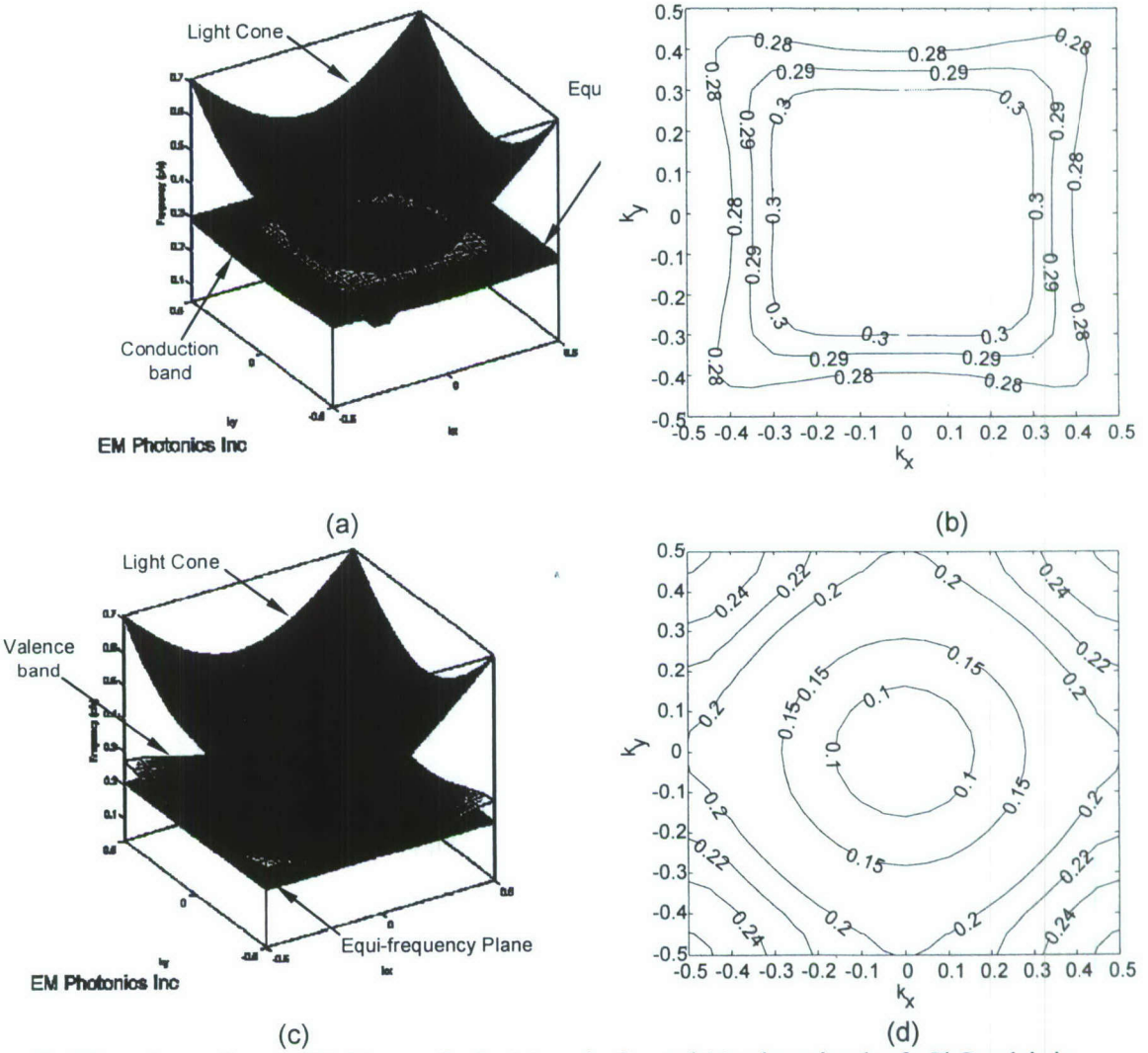
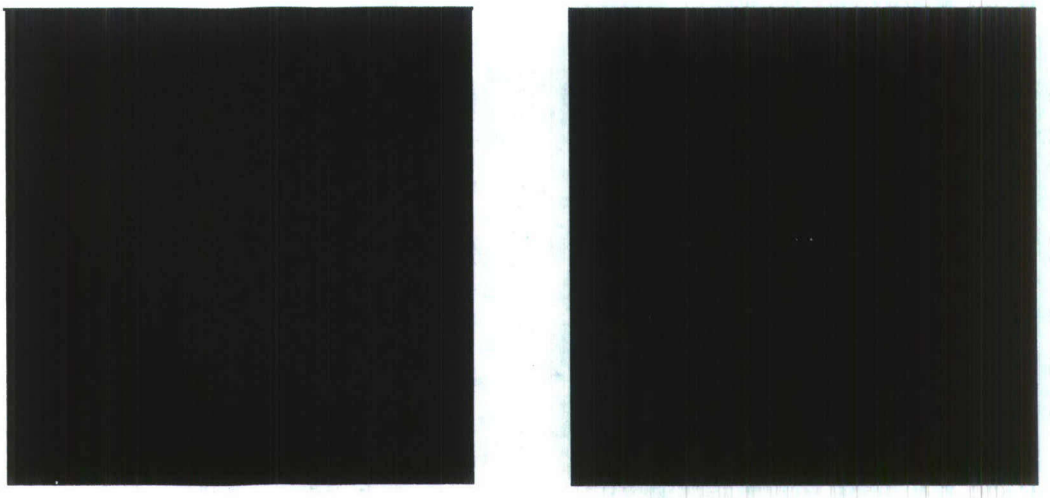


Figure 42 - Dispersion surfaces and light cones for the (a) conduction and (c) valence bands of a PhC and their respective EFCs in (b) and (d).

To illustrate the self-collimation phenomenon, we simulated using the FDTD method a point source located inside two structures with different EFCs: a homogeneous silicon slab, and one perforated by a square lattice of air holes, with r/a = 0.3. For the homogeneous material, the EFC is a circle, and therefore light waves emanate from the source and propagate isotropically within the plane as shown in Figure 43(a). On the other hand, if the EFC is nearly square, wave propagation due to a point source located at the center of the PhC lattice, as in Figure 43(b), is limited to the x- and y-directions.



(a) (b)

Figure 44 - FDTD simulation of an electromagnetic light wave emanating form a point source when placed in a (a) homogeneous (unpatterned) silicon slab and (b) a silicon slab perforated by a PhC consisting of a square lattice of air holes, wherein r/a = 0.3.

While self-collimation can be clearly observed theoretically by introducing a point source into the center of a PhC lattice, this is difficult to achieve in the optical regime except by embedding a source in a PhC consisting of an active material. Therefore, in order to experimentally observe the self-collimation phenomenon in a PhC lattice fabricated in silicon, one must introduce the source in such a way that lateral confinement of the light can be observed. In the next section, we demonstrate this capability by engineering the self-collimation properties of PhCs structures to design various applications

With this self-guiding lattice, we proceed to design an Electro-optic self collimation modulator in photonic crystals

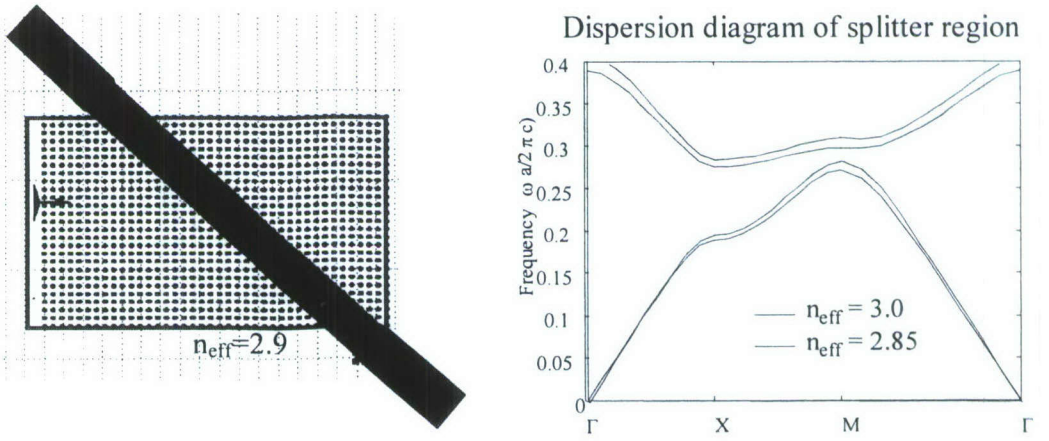


Figure 45 - (a) Schematic of modulator design with a = 450nm and D = 315.8nm in splitter area and a = 450nm and D = 270nm in guiding area. Green areas highlight locations of electrical connections to electrodes used to modulate the carried concentration in the splitter area. (b) Band diagram in the splitter area overlapped with band diagram of the background area.

4.5.1 EO-SCPhC Modulator Design and Analysis

The modulator consists of a hybrid photonic crystal structure shown in Figure 45. the structure combines a self collimation photonic crystal structure and a partially reflecting/transmitting structure. The diagonal rows have larger fill factor than the background photonic crystal structure and hence have a different spectral and spatial response. The lattice constants are same. Two electrodes, which are along the diagonal direction, are used to inject current for modifying the effective index of diagonal PhCs. When there is no injected current, the photonic crystal structure work as self-collimation waveguide, and the splitting region works slightly above the band gap, as shown in Figure 46(b). The input light passes the splitting area as shown in Figure 46 (a). When the current is injected, the free carrier concentration changes the refractive index. The change in effective index shifts the dispersion diagram of the diagonal PhCs as shown by the red lines in Figure 46(b). when the frequency of input light falls in the band gap region, the input light is reflected by the diagonal PhCs. Figure 46 shows the simulation results when the effective index changes. As we can see, when the effective index changes from 3 to 2.8, the input light changes from transmission to reflection

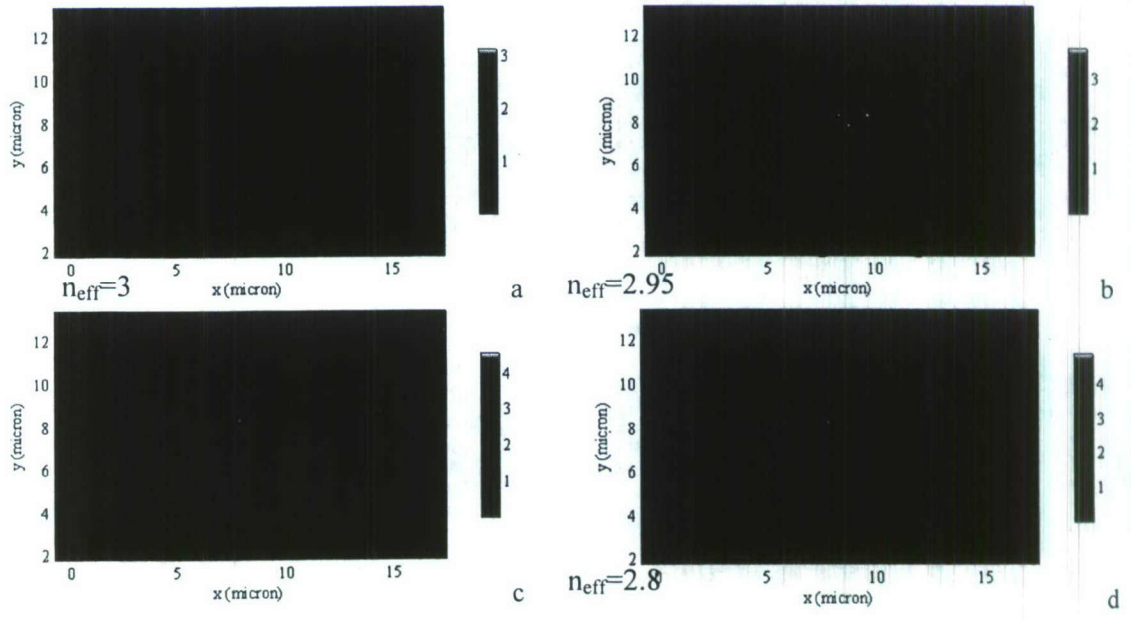


Figure 46 -Simulation results of PhC modulator with different effective index of diagonal PhCs.

4.5.2 Determining the Appropriate Doping Concentrations (Silvaco)

To properly simulate the underlying electrical mechanisms that govern the operation of the current injection based modulator, the software package, Silvaco, was purchased. The initial simulation work entailed using a 2D approximation of the diode structure, shown in Figure 47. In the vertical direction, the device was composed of a 260 nm thick layer of silicon on top of a 1 μm thick layer of SiO_2, and in the horizontal direction, the model contained two highly doped regions, 10^{20} /cm^{3}for the source and drain, separated by 5 μm of a much lower doped intrinsic region, $p = 6\times10^{14}$.

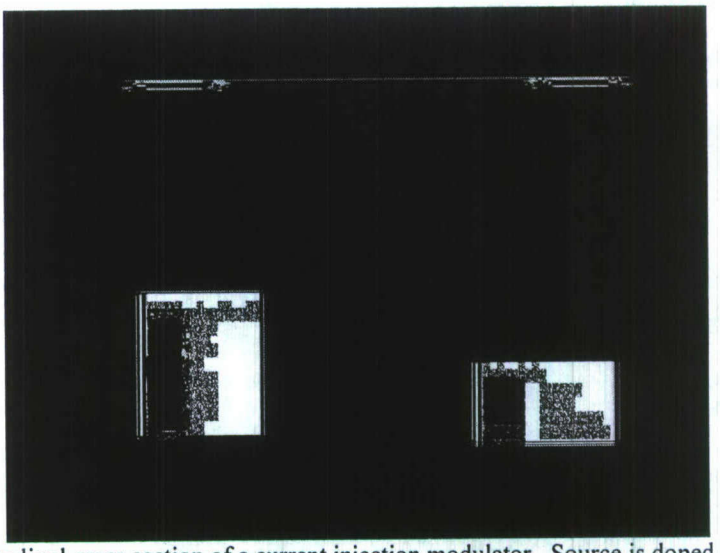
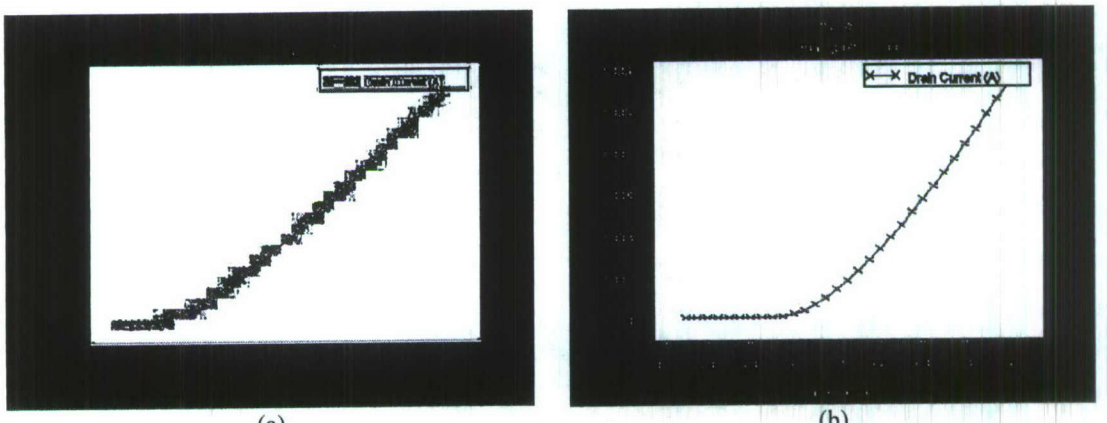


Figure 47 - Longitudinal cross section of a current injection modulator. Source is doped P+ and intrinsic section is doped P-. The drain is p+ for p-i-p diode and n+ for p-i-n diode.

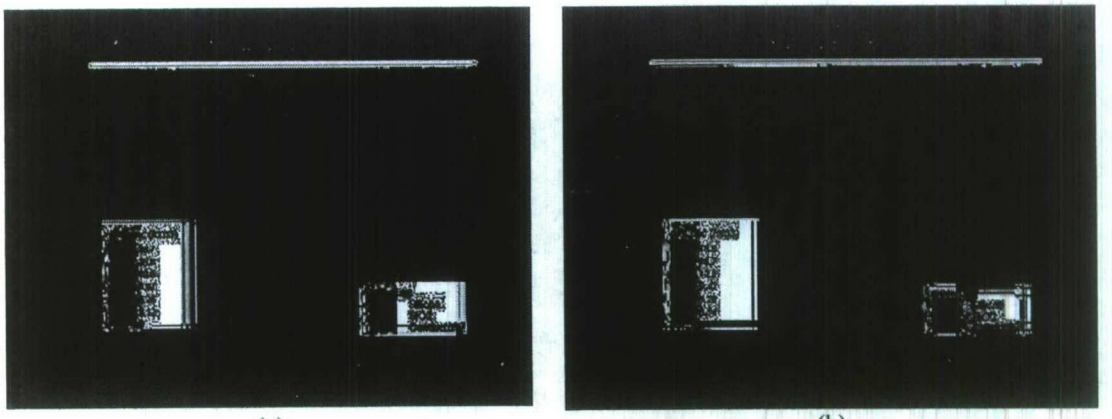
4.5.3 P-i-P/P-i-N Device Simulations

The first type of electrode simulated was the P-i-P diode, which has already been fabricated. As shown in Figure 48(a), the results indicated that the turn on voltage was around 8V and the drain current reached 100 uA at a drain-source voltage of 50 V. While the turn on voltage was approximately close to that of the fabricated device, the drain current was not. Further investigation is needed to resolve this discrepancy; however, a much more promising structure was the P-i-N diode. In this configuration, the drain was doped with an n-type dopant instead of p-type as in the P-i-P structure. As shown in Figure 48(b), the I-V characteristics were much closer to that of a PN diode. The results indicated a much higher drain current of 5 mA at around 1.8 V. This level of current has produced modulation in the fabricated P-i-P diode, but at 50 V. By switching to an n-type dopant, the required driving voltage has been lowered to a much more manageable level.



(a) (b)

Figure 48 - Plot of drain current vs. drain-source voltage. a) p-i-p diode. b) p-i-n diode.

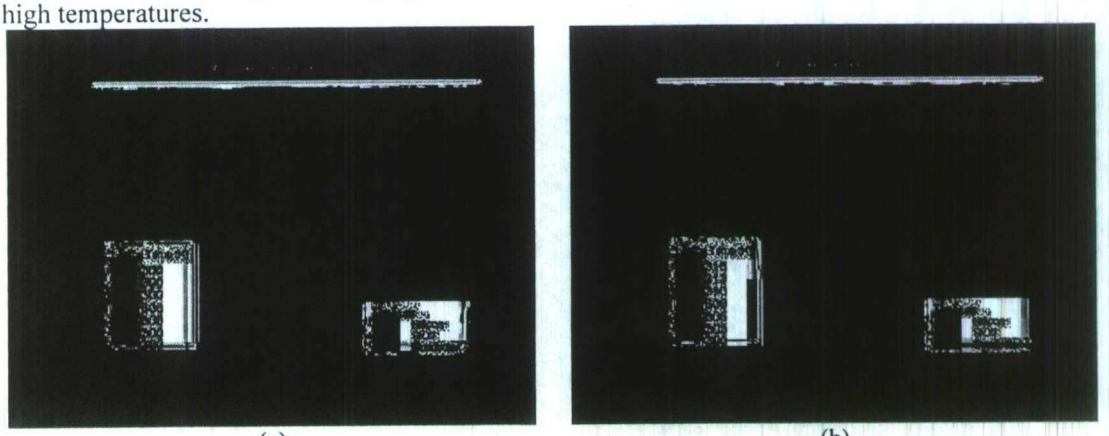


(a) (b)

Figure 49 - Plot of electron concentration. a) Drain voltage is .1 V. Intrinsic region indicates a concentration of 1014 /cm3. b) Drain voltage is 1.8 V. The electron concentration in the intrinsic region has increased to 1019 /cm3.

Additional testing as shown in Figure 49 revealed the electron/hole concentration for two different driving voltages. At .1 V as seen in Figure 49(a), the P-i-N diode was biased below turn-on, and the resulting e/h concentration was 10^{14} /cm^3. At this level, no measurable refractive index change was realized. At 1.8 V as seen in Figure 49(b), the e/h concentration increased to a much higher 10^{19} /cm^3 which modulated the index by about $\Delta n = 0.02$. This is promising; however, more work is needed to increase this concentration to even higher levels for greater index modulation.

The last simulation performed was a simulation of the lattice temperature. The thermal-optic effect is one that counters the refractive index change realized by free carrier injection, so an accurate model of the lattice temperature is desirable. In the first case as shown in Figure 50(a), the intrinsic region temperature increased by less than half a degree K when the drain-source was biased at 1.8 V. When the source-drain bias was increased to 5 V, the temperature difference was only 16 K. This is very encouraging as the electric-optical effect only becomes important at very high temperatures.



(a) (b)

Figure 50 - Plot of steady state lattice temperature. a) Drain voltage is 1.8 V and max temperature is 300.4 K. b) Drain voltage increased to 5 V and max lattice temperature is barely above 316 K.

4.6 EO-SCPhC Modulator Prototype Fabrication and Characterization

4.6.1 Prototype Fabrication

We fabricated the modulator as shown in Figure 51. We tested the devices in NIR setup. However, when the current is injected through the electrodes, we were not able to observe any light propagation through the device. It may be caused by low doping concentration (1e18).

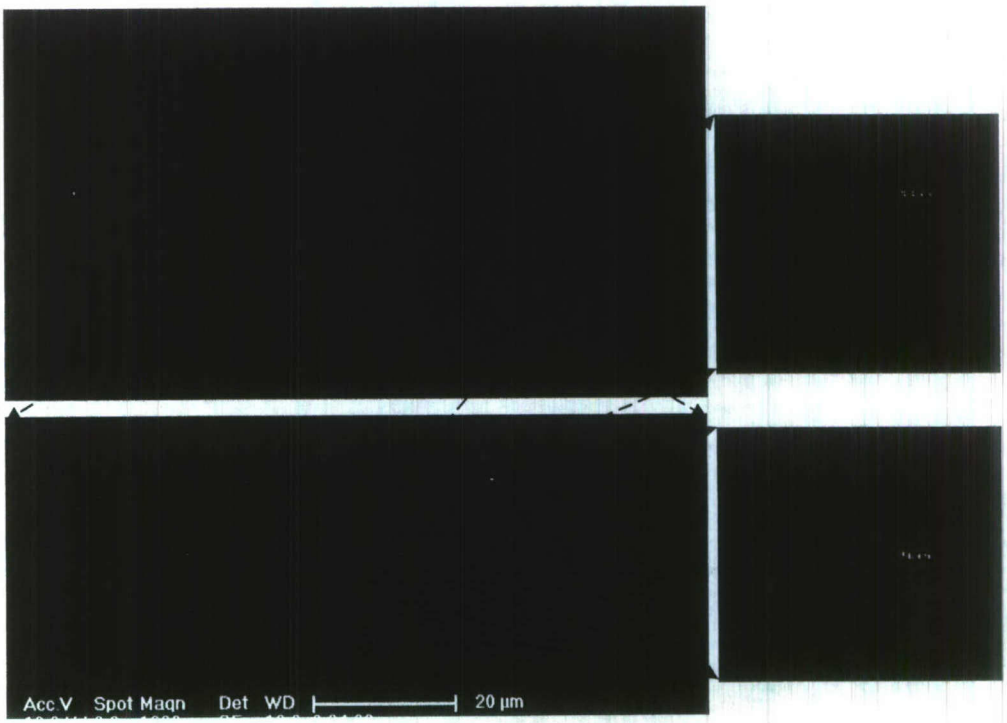


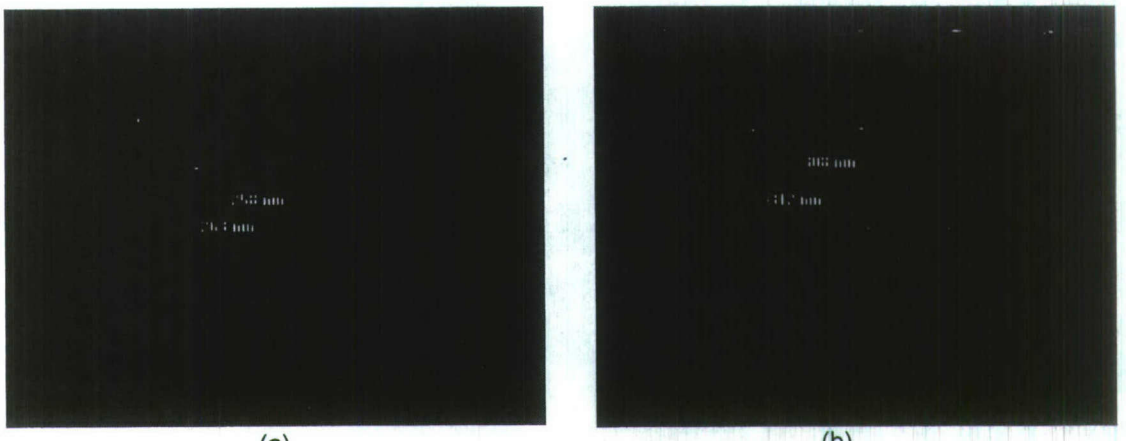
Figure 51 - Top view of fabricated SCPhC silicon based modulator

Using the device simulation results presented in the previous section, we proceeded to fabricating a prototype to validate the numerical results obtained. This involved improving upon every aspect of the fabrication process used to fabricate the PIP diodes to ensure that the devices were reproducible and the dimensions kept intact so that operation approaching 1 GHz can be obtained. To this end, the advances and the current problems are outlined here.

The first processing step investigated was the e-beam lithography which defines the sub-micron photonic crystal and the associated waveguides which couple light into and out of the structure. In the past the Raith 50 e-beam writer along with PMMA resist has produced adequate results for fabricating PhCs. However, there is always the desire to see how well the PhC pore diameter and eccentricity can be controlled. To this end, the use of Zep520 was investigated as an alternative to PMMA because it requires a lower exposure dose and is a more resistant to degradation during the subsequent etching. These two properties will allow a smaller beam size to write the PhC, which should allow finer control over the size of the PhC pores.

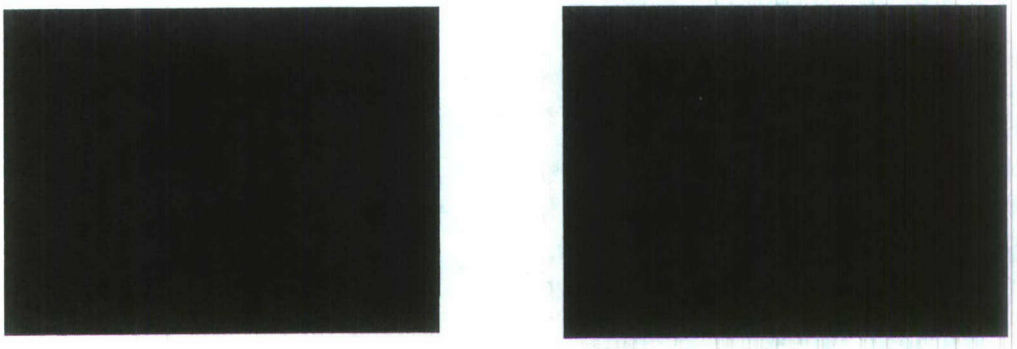
To investigate the performance of Zep520, an array of square PhC lattices, all with lattice spacing of 450 nm, was written into a 300 nm thick layer of resist and imaged. The variation in the dose investigated was 12 $\mu C/cm^2$ to 96 $\mu C/cm^2$ in steps of 12 $\mu C/cm^2$, and the radius of the

pores was varied from 90 nm to 170 nm in increments of 10 nm. Two such PhC lattices produced are shown in Figure 52. With a design radius of 110 nm and a dose of 60 uC/cm2, the developed holes enlarged to 260 nm in diameter. Shown in fig. 1b, was the result of a lattice exposed with a radius of 130 nm and a dose of 60μC/cm2, which enlarged to 310 nm in diameter. Both of those these lattices are important for the design of the PIN PhC modulator, as the 270 nm holes support self collimation, and the 310 nm holes create a band gap when the surrounding index is lowered through current injection. The second important result from this investigation was that of the hole eccentricity in both cases shown in Figure 52 was lower than 3% which is a very low value. This value is important to keep as low as possible so that the dispersion diagrams of the fabricated sample stay as close as possible to the simulated case.



(a) (b)

Figure 52 – a). Square lattice PhC fabricated in 300 nm thick Zep520 with a designed hole diameter of 220 nm and a dose of 60 μC/cm2. b) Same as 1a with an increase in the hole diameter to 260 nm.



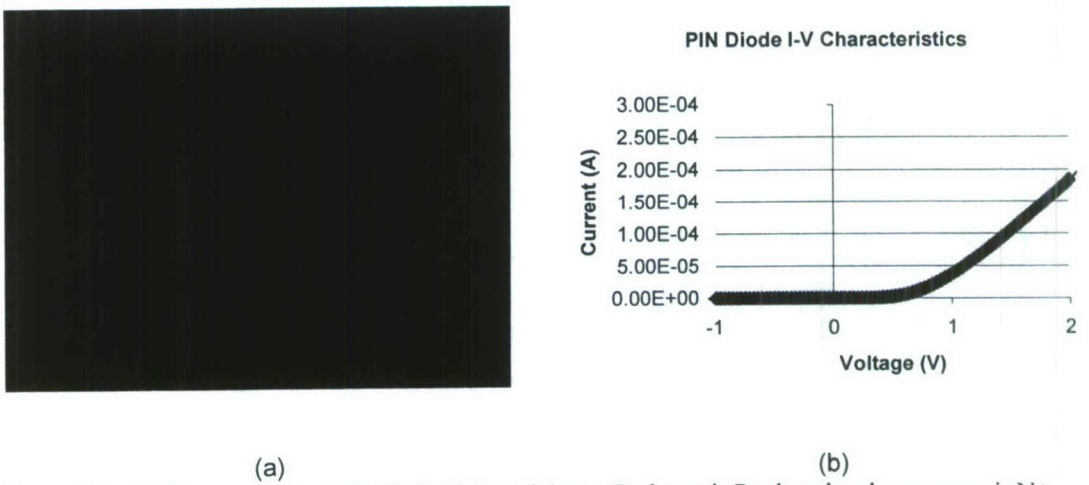
(a) (b)

Figure 53 – a) N type SOD spun onto a silicon wafer in an air atmosphere. b) N type SOD spun onto a silicon wafer in a solvent atmosphere.

The next phase of the fabrication process developed was the diffusion of the N+ doped region. In the previously fabricated PIP diode, both electrodes were placed upon P+ type doped regions. This was done to facilitate ease of alignment as well as simplify the fabrication process. Additionally, the N type spin on diffusant (SOD) proved initially to be problematic to use. This was a result of the different solvents comprising the bulk of the SOD which turned out to be very different from that used in the P type SOD. When the N+ type dopant was spun on the substrate in the presence of air, the glass dried in clumps which can be seen in Figure 53(a). These clumps would then during the subsequent drive in deposition, deposit the N+ dopant unevenly and cause

poor device reproducibility. To overcome this, a process was developed where the N+ dopant was spun in a solvent rich environment, in this case isopropyl alcohol, which prevented the formation of glass islands and promote a more uniform layer. This in turn provided reproducible results when the surface resistivity was measured. The improvement in the layer uniformity can be seen in Figure 53(b). However, the change in the surface color was a result of the high temperature curing process which was not performed for the sample in Figure 53(a). Overall, for a 30 minute diffusion at 1050°C, the surface resistivity for a 260 nm thick silicon device layer was around 30 ohm/square. This is roughly half the value for P type SOD after a similar 60 minute diffusion, and is a result of phosphorus' much higher diffusion coefficient as compared to boron.

Upon completion of a process for diffusing N type dopants into silicon, actual PIN diodes were designed and fabricated. Initially the design mirrored that of the previously fabricated PIP diodes. In this case, the PhC on 260 nm thick SOI was designed around a square lattice self collimating region of 270 nm diameter air holes with a lattice spacing of 450 nm, and a square lattice splitting region of air holes increased to 310 nm in diameter. On either side of the active modulation region, doped regions 3-4 um in width were placed to provide carrier injection under forward bias. In the case of the PIN junction, each doped region was fabricated separately as one was P type and the other N type. A picture of a fabricated junction is shown in Figure 54(a) and the electrical I-V characteristics shown in Figure 54(b).



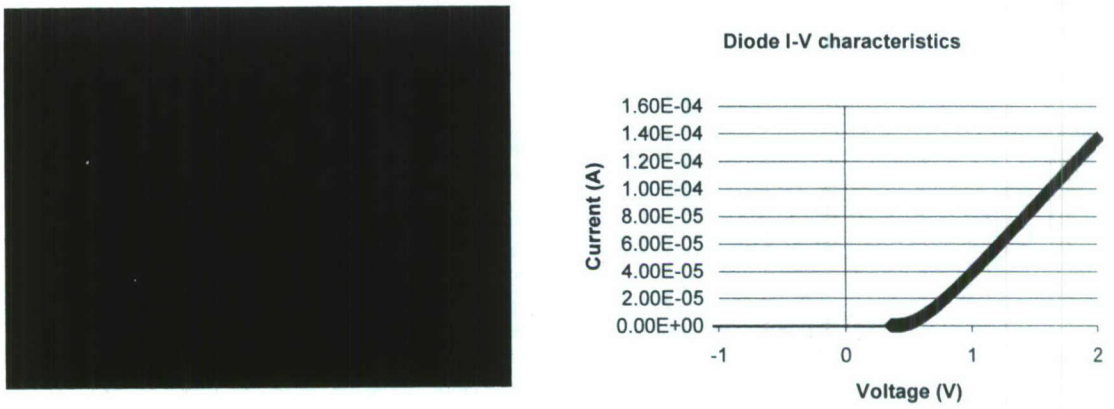
(a) (b)

Figure 54 – a) First generation PIN diode PhC modulator. Red area is P+ doped and green area is N+ doped. b) I-V characteristics of device shown in a).

As shown in Figure 54(b), the I-V curve represented very closely that of a standard PN junction with a threshold voltage of 0.6V. What is also shown was the immediate change in the curve from non linear PN junction behavior to linear behavior of a resistor as the voltage rose above 1V. This can be explained by the large series resistance present because of the placement of the gold contacts over 100 μm away from the actual PIN junction. This was necessitated by the design because the doped areas were very narrow and made placing gold wires above them very difficult. Since the resistance of the P type area was approximately 60-100 ohms/square and the resistance of the N type region roughly half this, one can see that the resistance added up when the doped regions were 30 squares in length or more.

To overcome this series resistance, a new design was created with doped regions 40 μm in width until the last 20 μm where the stripes narrowed to 5 um as shown in Figure 55(a). Above the 40 μm wide doped regions, gold stripes were placed to lower the series resistance to negligible values until the last 5μm. As shown in Figure 55(b), the series resistance didn't reduce

but rather increased in magnitude as the current dropped to 140μA at 2V. This is counter intuitive as clearly the graph indicates the presence of series resistance as shown by the linear behavior above 0.7V. This means further analysis is need to determine the root cause of this limiting behavior, because the required amount of current needed to modulate the incoming signal is on the order of a couple mA.



(a) (b)

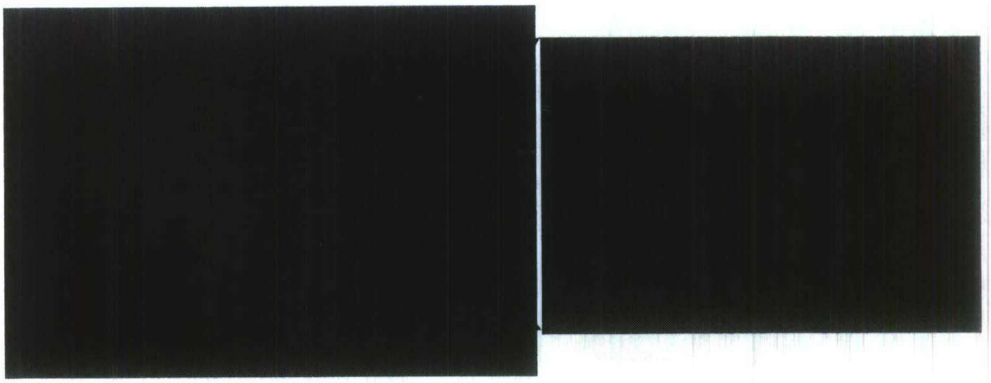
Figure 55 – a). PIN diode PhC modulator with enlarged electrodes to reduce series resistance. b). I-V characteristics of device shown in a).

In conclusion, several fabrication processes were improved upon to facilitate the reproducible fabrication of PIN junctions. After initial testing, it was determined that the junctions displayed high series resistance. To combat this electrodes with lower resistance were fabricated, although this had negligible impact on the I-V characteristics of the device. In the end, more work is needed to lower the performance limiting resistive behavior.

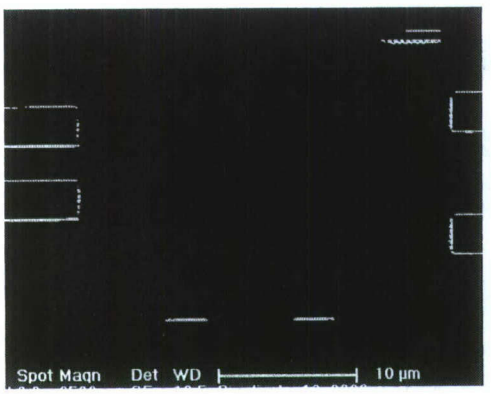
4.6.2 Modified Design

New design of the SCPhC modulator were fabricated as shown in Figure 37. The microscope images of one fabricated device are shown in Figure 56 (a). The doping regions, metal contacts, and photonic crystals can be seen clearly from the zoom in image at the right hand side. Figure 56(b) and (c) shows SEM images of photonic crystal areas. As we can see, for the device showing in the left figure, the doping area was inserted into the photonic crystal region to improve confinement of injecting carriers.

For the device shown in right figure, several trenches were etched around the photonic crystal region. These trenches prohibit the injected carriers passing through the open photonic crystals. And they help to reduce the leak of injection current, and increase the quantum of carriers which pass through the diagonal splitter.



(a)



(b)

(c)

Figure 56 - (a) Microscope images of fabricated modified modulator design. The pink regions are doping areas; the yellow regions are metal contacts. (b), (c) SEM top views of the devices after ICP etching. Extending the doping region and etched trenches help to constrict the injected carriers through diagonal areas.

4.6.3 Prototype Characterization

The fabricated device was tested on the optical bench. Figure 57 shows the top-view images of PhC regions captured by an IR camera when the applied voltages are 0V, 30V, and 50V, respectively. From the figures, we can clearly observe that the intensity of output light reduces when the applied voltage increases.

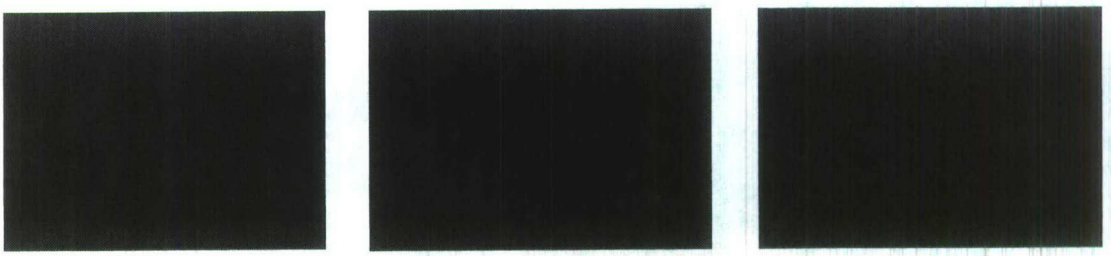


Figure 57 - IR images of the device when the applied voltage is at (a) 0V, (b) 30v, and (c) 50V

The output light was collected by a lensed fiber and measured by a photo detector. Figure 58 shows the measured output light at λ = 1428nm in a time scale, where each time step indicates 500ms. The shaded area shows the time regions when 40V voltage was applied. As we can see from the graph, the output light dropped corresponding to the applied voltage, and resumed when the applied voltage was switched off. The spectra of the output light at different applied voltage was also measured and shown in Figure 58

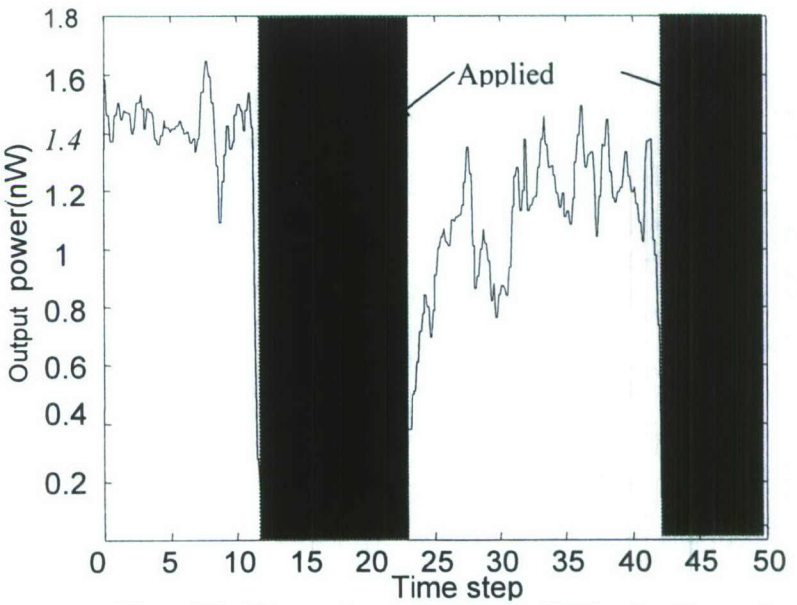


Figure 58 - Measured output light at λ = 1428nm in a time scale.

Figure 59 shows the captured top view images during the test of devices with modified design. Since photonic crystals need to be released for TE mode self-collimation. The narrow input waveguides were release as well. Wile the sample was bonding, the ultrasonic vibration of the bonding needle broke the input waveguide.

In order to test the fabricated devices, we launched the laser beam to the output waveguide and observed the behavior of the devices through the scattering light from the photonic crystals.

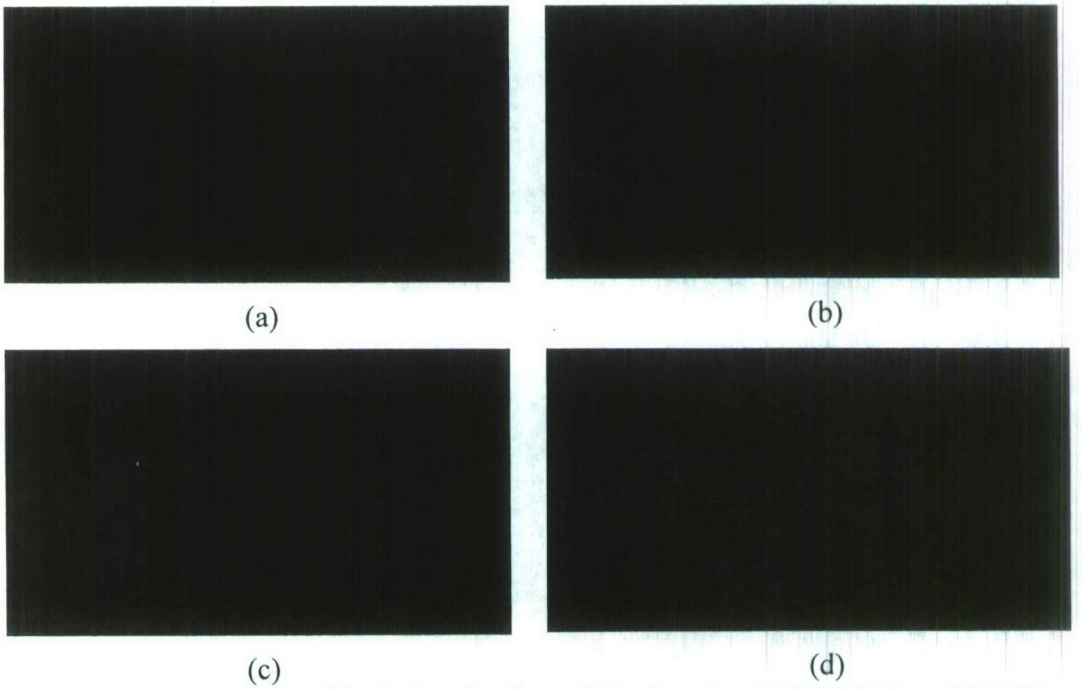


Figure 59 - IR images of the device when the applied voltage is at (a) 0V, (b) 25v, and (c) 45V

5 Si-based SCPhC Switch

Electro-optical switches are key components of such photonic integrated circuits, yet only one proposal for implementing such switches--a resonator device--has appeared in the literature. [8] In this paper we present the conception, numerical analysis of a dispersion based photonic crystal switch that utilizes electrically or optically induced loss (conductivity). To our knowledge, this is the first dispersion based photonic crystal switch that has been proposed and analyzed.

5.1 Initial Design

In the previous section we demonstrated how self-collimating photonic crystal lattice with additional, strategically placed modifications, can be used for efficient routing of optical signals on the chip scale. Such structures can be used as an interconnection fabric for on-chip communication, and offer dramatically improved bandwidth over their electronic counterparts. In this case, the interconnection topology is defined during the design stage and is literally etched into the underlying material used as a medium for optical transmission. As such, it is static, and cannot be reconfigured during the device operation. However, since the medium is silicon—a semiconductor, whose optical properties can be modified by injecting carriers, applying an external electric field, or high-intensity optical fields—one may contemplate designing optical switches that would allow dynamic

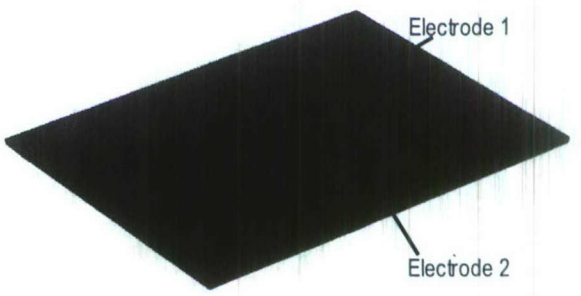


Figure 60 - A dispersion based optical switch featuring two orthogonal electrodes. Activating either electrode controls the direction over which the signal will travel.

interconnection-network reconfiguration. Thus, in this section, we introduce an optical switch, controlled electronically, and illustrate its use to define a reconfigurable 2 × 2 optical cross-connect network.

The self-collimating photonic crystal structure is designed so that when an external electric field is applied, with electrodes deposited on silicon, the resulting change in the dielectric constant modifies the dispersion properties of the lattice, and produces a virtual mirror as shown in Figure 60. By controlling the region where the electric field is introduced with properly placed and shaped electrodes, we can decide if and how the propagation of light in the photonic crystal is affected. Figure 43 shows steady-state results for our dispersion-based switch, which can exist in three distinct states: ON, OFF, and PASS.

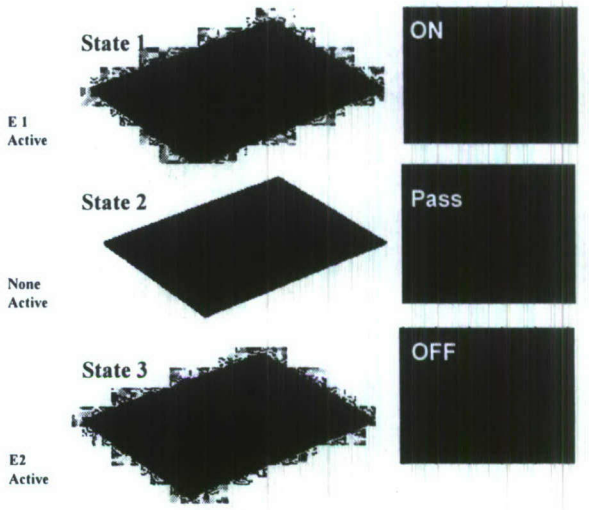


Figure 61 - Steady state results for the switch. Switch shown in three different states ON (state when electrode E1 is active), PASS state (when neither E1 nor E2 are active), and OFF (state when E2 is active) .

The device of Figure 61 can be interconnected and cascaded in the forward direction into an N × N optical cross-connect network. An example of such network is a 2 × 2 routing structure shown in Figure 62, which utilizes 4-PN junctions that can be tuned to modulate the refractive

index under the highlighted areas

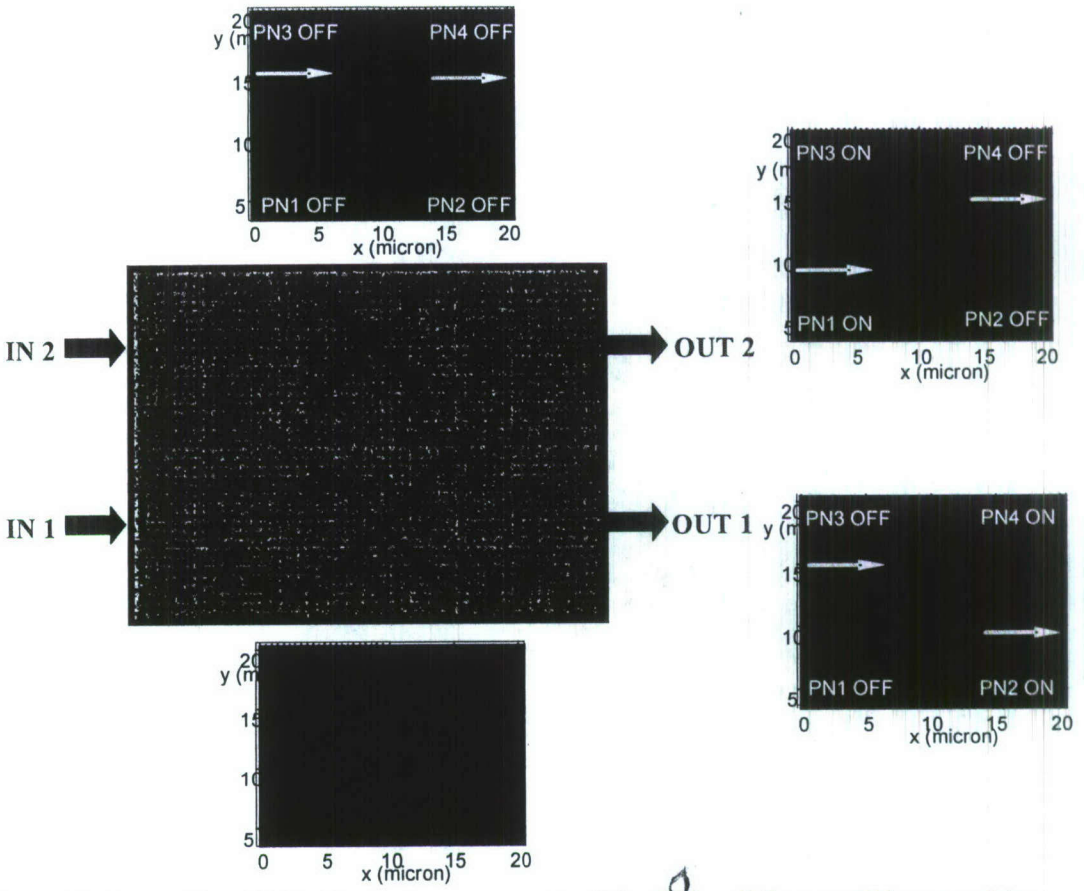


Figure 62 -A reconfigurable 2 × 2 optical cross-connect switch utilizing all three possible states of the virtual mirror.

solution for a 2 × 2 cross-connect, which uses three virtual and three fixed mirrors, and allows for both signals to be transmitted simultaneously, is shown in Figure 63.

E1	E2	E3	IN-OUT
OFF	ON	ON	1-1, 2-2
ON	OFF	OFF	1-2, 2-1

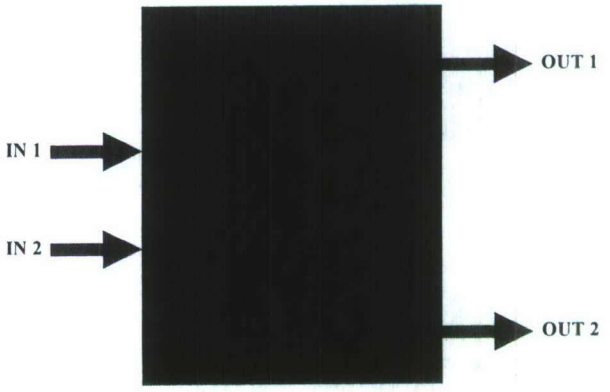


Figure 63 - A reconfigurable 2 × 2 optical cross-connect switch allowing for simultaneous transmission of both signals.

5.2 Mach-Zehnder Design

Mach-Zehnder interferometers (MZI) have been shown to work as effective optical switching elements with high sensitivities. A phase shift induced by a modulation in refractive index in one branch of the switch will change the output power due to the interference of the coherent beams. The output power, P_T, of this switch relative to the input power, P_0, is given by

$$\frac{P_T}{P_0} = \cos^2\left(\frac{\Delta\varphi}{2}\right). \tag{1}$$

The interferometer phase, $\Delta\phi$, is given by

$$\Delta\varphi = \frac{2\pi\left(n_{eff_s}L_s - n_{eff_r}L_r\right)}{\lambda_0}, \tag{2}$$

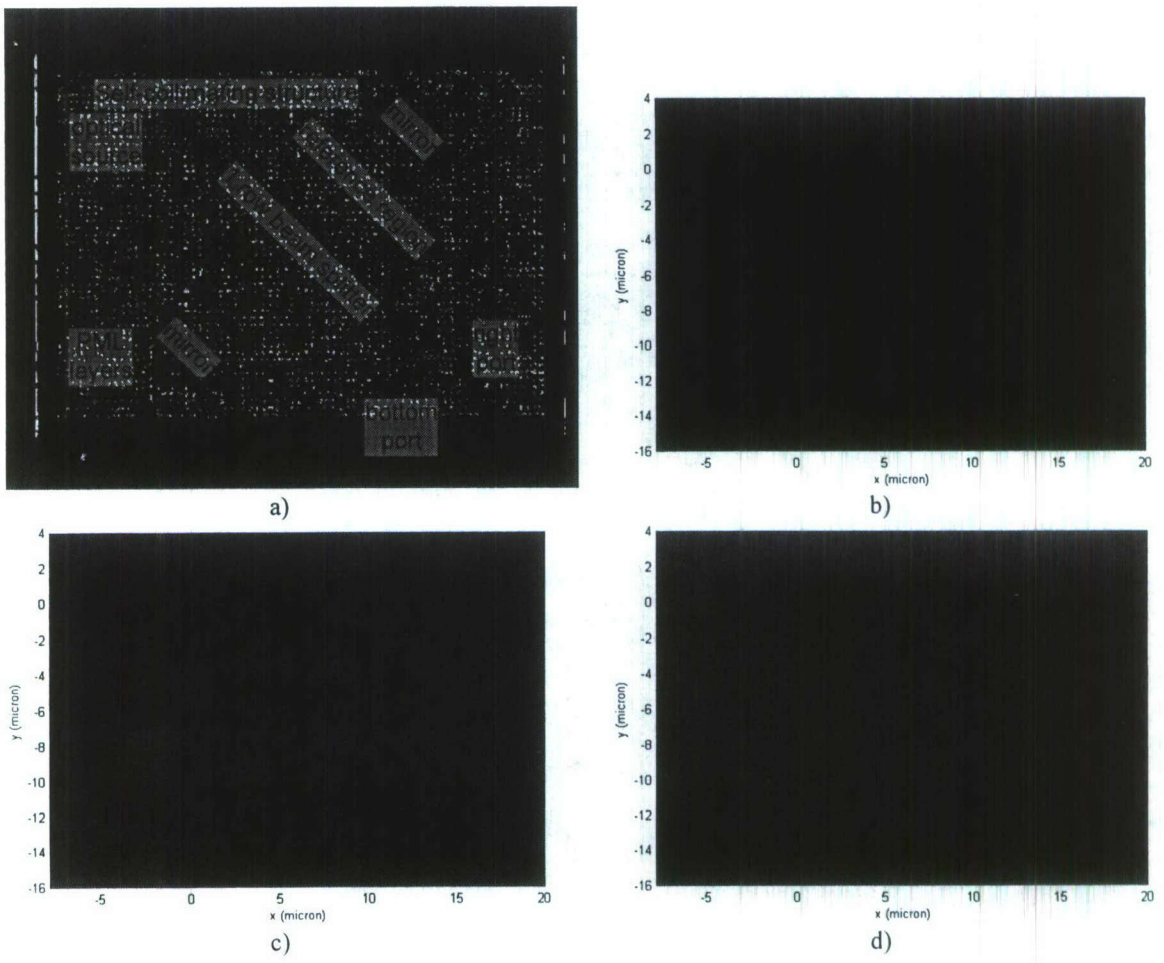


Figure 64 - a) Mach-Zehnder switch structure with a beam splitter and mirrors embedded in a self-collimating photonic crystal structure. A 2 μm wide TE Gaussian beam with a wavelength of 1.538 μm (normalized frequency, $a/\lambda = 0.26$) is launched from the left of the structure. b)-d) Steady state amplitude plots for the switch as the refractive index in the columns of the lower half of the switch is varied from b) 1.0 (i.e. balanced MZI), c) 1.1, and d) 1.2.

where $n_{eff(s,r)}$ and $L_{(s,r)}$ are the effective refractive indexes and physical length of the switch and reference branches, respectively. The term in parenthesis in equation 2 is the difference in optical path length between the two paths of the interferometer. The change in the interferometer phase as a function of change in effective index is

$$\frac{dn_{eff}}{d\varphi} = \frac{\lambda_0}{2\pi l_s}, \tag{3}$$

where l_s is the length of the segment where the switch waveguide is influenced by the external modulation of the refractive index. Photonic crystal (PhC) structures enable the manipulation and guiding of optical signals in microscale dimensions. In this project, we analyze the use of photonic crystal structures to perform self-collimation and beam splitting to enable the fabrication of very dense, parallel Mach-Zehnder optical switchs.

A very compact Mach-Zehnder interferometer can be fabricated by combining self-collimation, two 1:1 beam splitters, and two fully reflecting mirrors. A diagram of the interferometer is shown in Figure 64(a). The bulk of the switch is comprised of the self-collimating structure with a lattice constant of 400 nm and radius of 104 nm. A 1 row beam splitter with a hole radius of 166 nm (0.415*a*) designed to equally split the optical signal cuts diagonally through device. Two photonic crystal mirrors with a hole radius of 152 nm (0.38*a*) in the upper right and lower left corners direct the beams to the output port. the output of the MZI is dependant on the relative phases of the two signals. The phase shift, and hence the sensitivity of the interferometer, is proportional to the change in effective index and the length of the interaction, l_s. If half of the MZI is exposed to an external modulation of refractive index while the other half is isolated, the MZI can act as a relative refractive index switch. In this particular device, the area of the MZ is 12 μm per side with a path length of 24 μm per branch. These dimensions are approximately 3 orders of magnitude less than commercial integrated optic MZIs. The micron scale dimensions of the device allows for fabrication of low-weight, compact, dense, and highly parallel switches. Inherent in the size of the switch is the disadvantage of significantly reducing the minimum sensitivity attainable due to very short interaction lengths. This effective interaction length, and hence the sensitivity, could be increased significantly by using photonic crystal structures to slow down the propagation of the optical signal as proposed by Soljacic et. al. [9]

Figures 64 b)-d) show the steady state amplitude simulations of the MZ switch as the refractive index in the air columns of the lower part of the switch is varied from b) 1.0 (baseline), c) 1.1, and d) 1.2. A 2 μm Gaussian shaped TE optical beam with a wavelength of 1.538 μm was used as the source. The simulation area was 30 μm wide by 22 μm tall with a 10 nm (~ λ/150) cell size. This results in a mesh with 6.6 million nodes (3000 x 2200) that includes 100 layers (1 μm) of perfectly matching layers (PML) on each side.

The structure continues to self-collimate the signal in the switching leg of the interferometer because the EFCs maintain their square shape even if the refractive index in the columns varies. It is clear from Figure 64b that if the refractive index is equal in the columns of both legs of the switch the optical signal will exit to the right of the switch. If the refractive index in the index change region increases to 1.2 the signal will exit from the bottom (Figure 64d) of the switch and the output will be split between the two ports with indexes between these levels. Figure 65 is a plot of the relative power of the two output ports of the Mach-Zehnder switch as the refractive index in the lower part of the interferometer is varied.

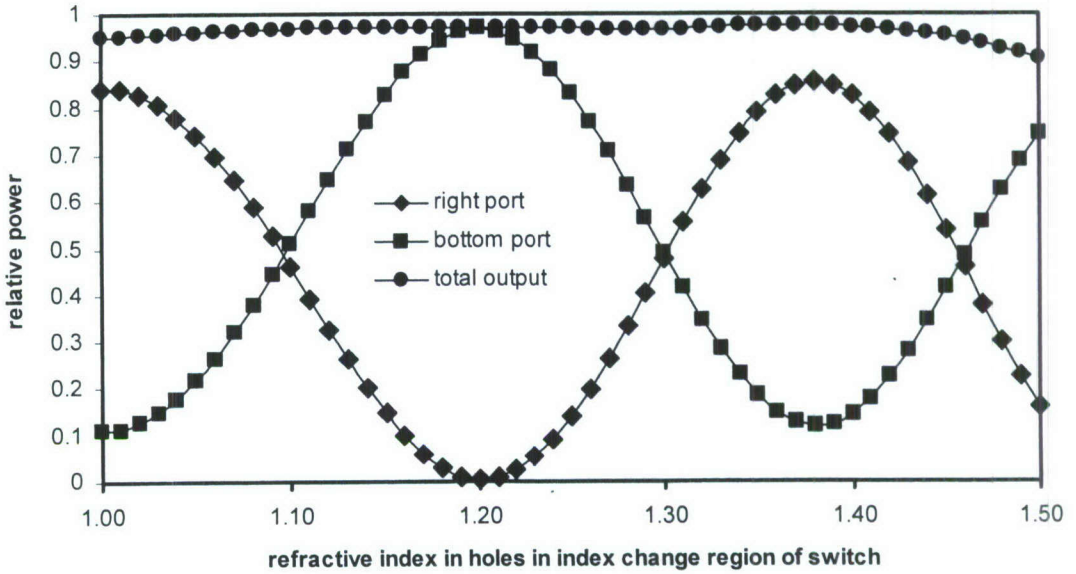


Figure 65 - Simulated performance of the MZ switch as the refractive index in the lower half of the device is varied.

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7 Publications

[1] Z. L. Lu, S. Y. Shi, J. A. Murakowski, G. J. Schneider, C. A. Schuetz, and D. W. Prather, "Experimental demonstration of self-collimation inside a three-dimensional photonic crystal," vol. 96, 2006.

[2] G. J. Schneider, E. D. Wetzel, J. A. Murakowski, and D. W. Prather, "Fabrication of three-dimensional Yablonovite photonic crystals by multiple-exposure UV interference lithography," *Proc. SPIE*, vol. 5720, pp. 9-17, 2005.

[3] D. W. Prather, S. Shi, S. Venkataraman, Z. Lu, J. Murakowski, and G. Schneider, "Self-collimation in 3D photonic crystals," *Proc. SPIE*, vol. 5733, pp. 84-93, 2005.

[4] S. Venkataraman, G. J. Schneider, J. Murakowski, S. Y. Shi, and D. W. Prather, "Fabrication of three-dimensional photonic crystals using silicon micromachining," *Applied Physics Letters*, vol. 85, pp. 2125-2127, 2004.

[5] S. Y. Shi, A. Sharkawy, C. H. Chen, D. M. Pustai, and D. W. Prather, "Dispersion-based beam splitter in photonic crystals," *Optics Letters*, vol. 29, pp. 617-619, 2004.

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9 New Discoveries

None

10 Honors/Awards

None